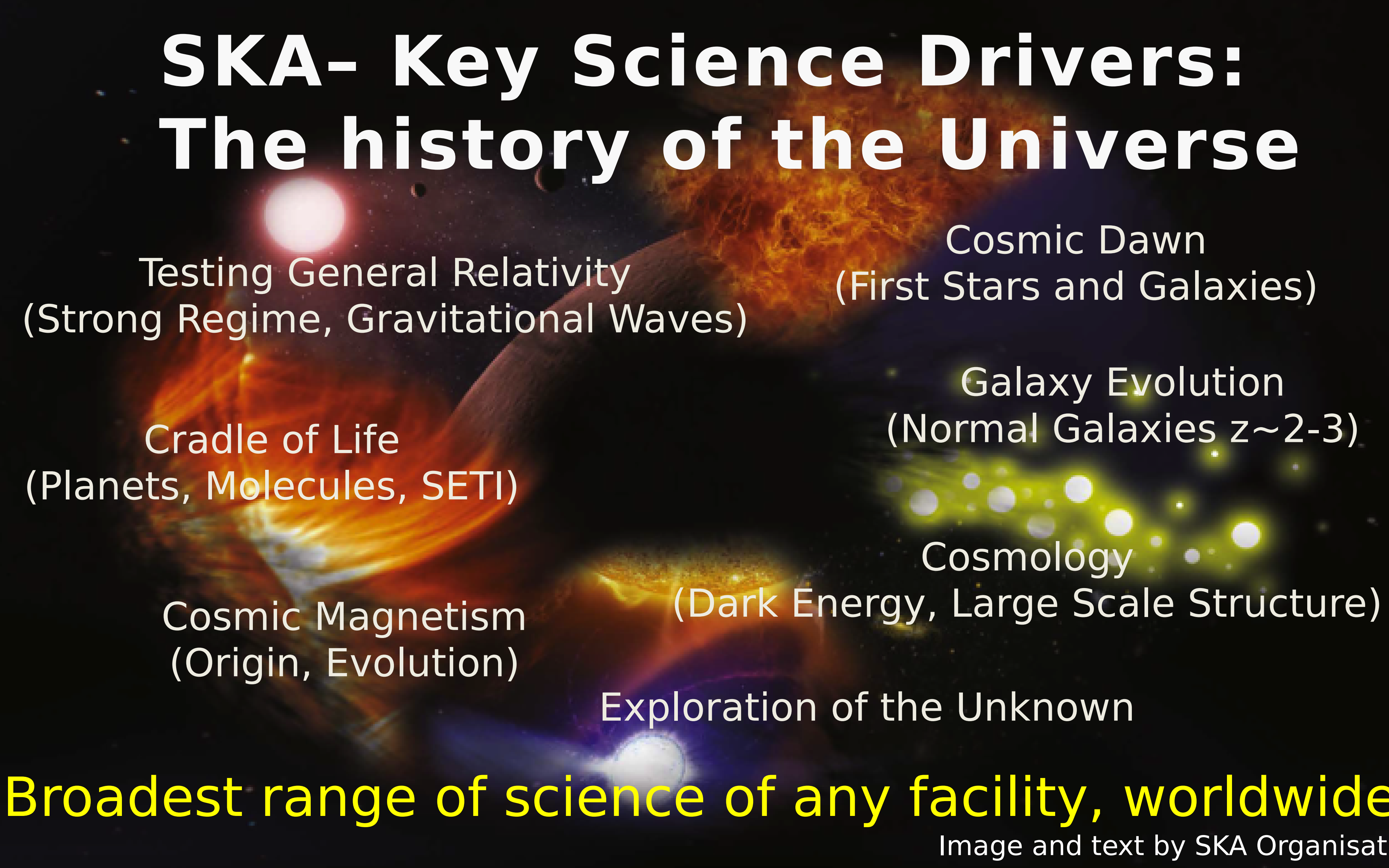
SKA
SKA AFRICA
SQUARE KILOMETRE ARRAY

SKARAB2

AUGUST 2017

Francois Kapp
(and the DBE team, particularly Adam and Jason)
(also using a few SKAO slides)

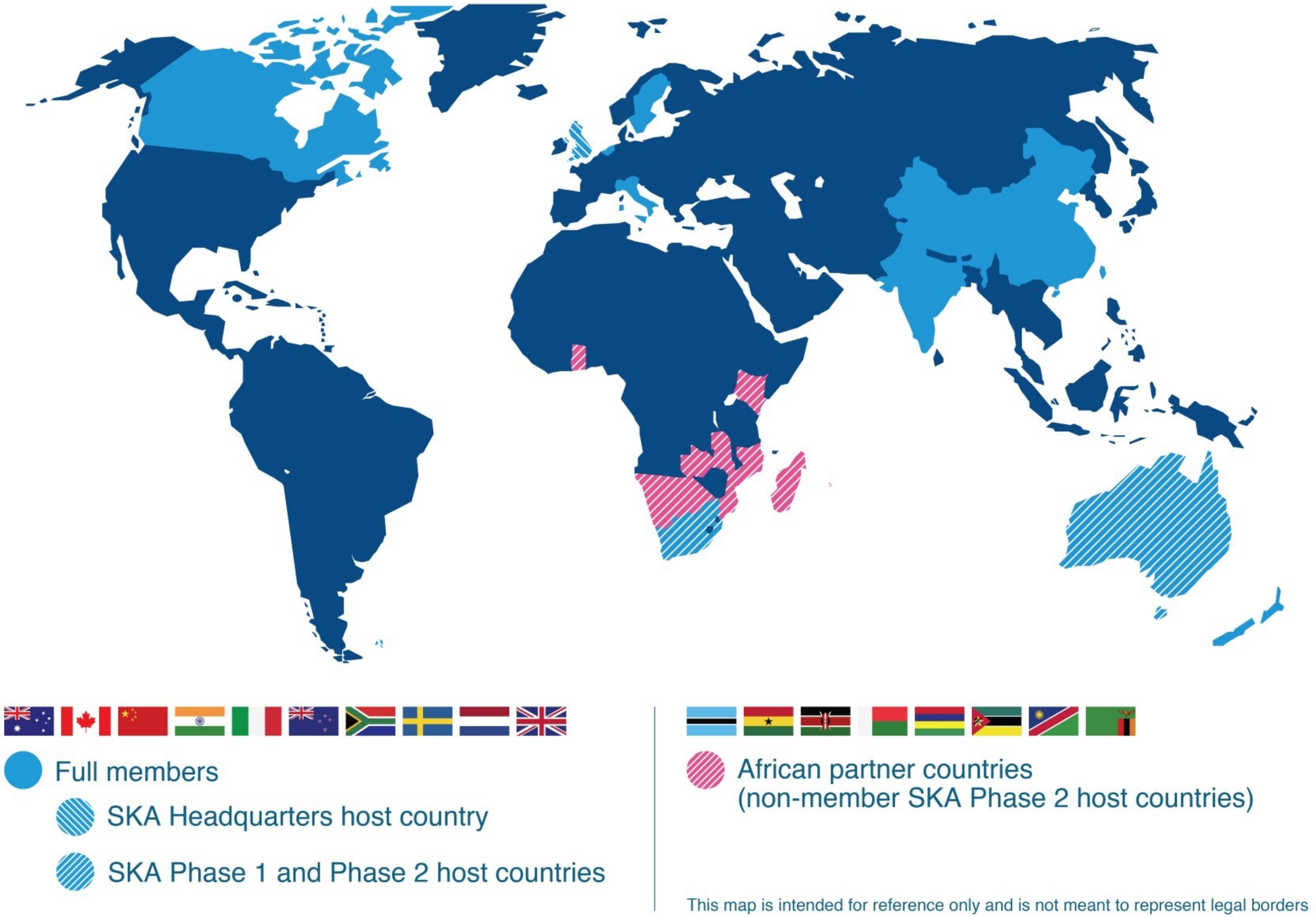

SKA– Key Science Drivers:
The history of the Universe
Testing General Relativity
(Strong Regime, Gravitational Waves)
Cosmic Dawn
(First Stars and Galaxies)
Galaxy Evolution
(Normal Galaxies z~2-3)
Cradle of Life
(Planets, Molecules, SETI)
Cosmology
(Dark Energy, Large Scale Structure)
Cosmic Magnetism
(Origin, Evolution)
Exploration of the Unknown
Broadest range of science of any facility, worldwide
Image and text by SKA Organisat

Square Kilometre Array

Overview

- 3 sites: 2 telescopes + HQ = 1 Observatory
- Now in design Phase: ~ €200M; 600 scientists + engineers
- Phase 1
  - Construction: 2019 – 2024
  - Construction cost cap: €674.1M (inflation-adjusted)
  - Operations planning now underway
  - MeerKat integrated
  - Observatory Development Programme
  - SKA Regional centres (locally funded)

- Phase 2: start mid-2020s
  - Advanced Instrumentation Program to mature relevant technologies now
  - ~2000 dishes across 3500km of Southern Africa
  - Major expansion of SKA1-Low across Western Australia



Full members
SKA Headquarters host country
SKA Phase 1 and Phase 2 host countries
African partner countries
(non-member SKA Phase 2 host countries)
This map is intended for reference only and is not meant to represent legal borders

SKA HQ in UK

Jodrell Bank
Discovery Centre
Lovell Telescope &...
Lovell Telescope
Bluedot Festival
S K A Organisation
Google

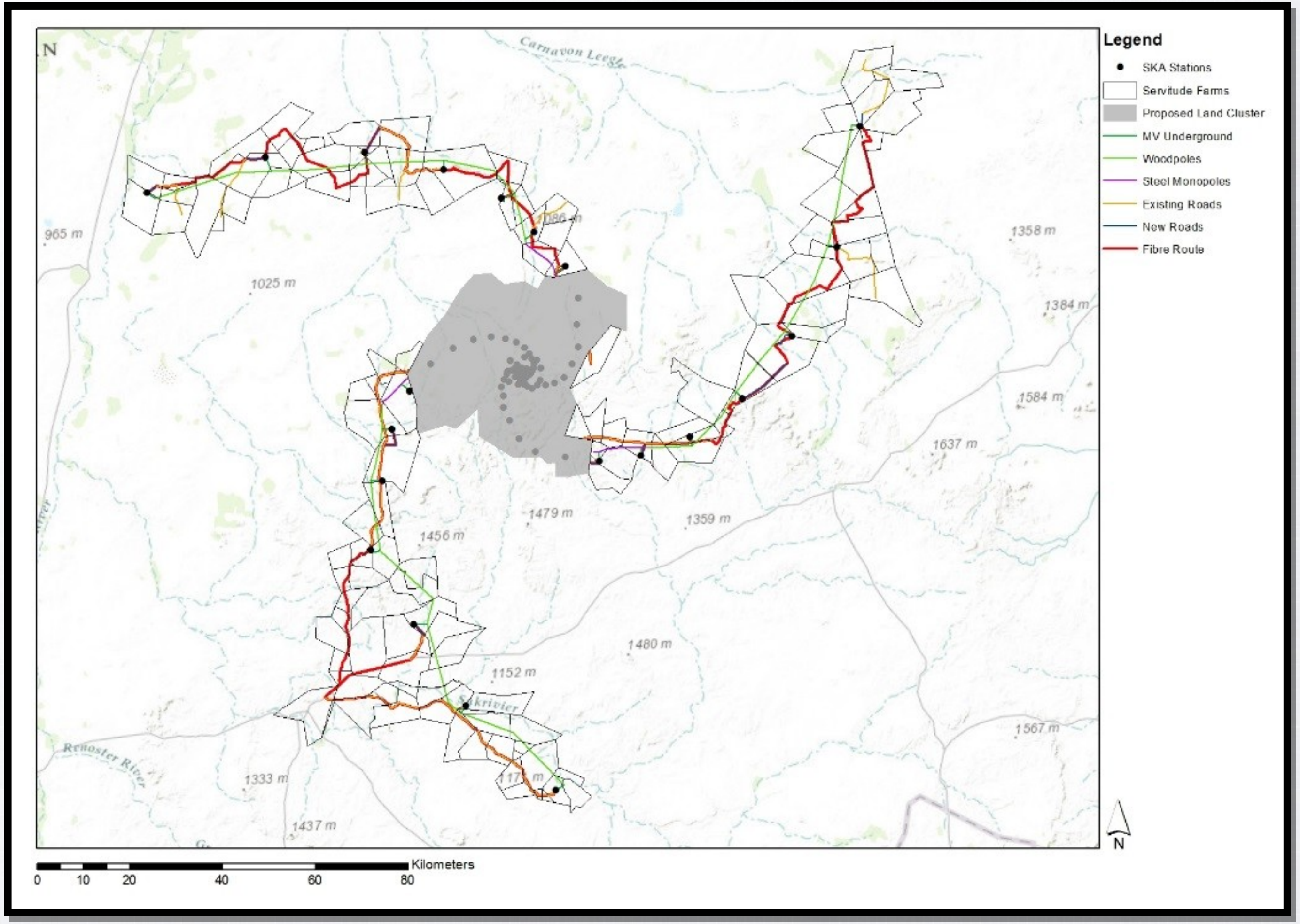
SKA telescopes in AUS & RSA

- SKA1-LOW
- 50 – 350 MHz
- Phase 1: ~130,000 antennas
- across 40 - 50km

- SKA1-Mid:
- 350 MHz – 24 GHz
- Phase 1: 130 15-m dishes across 120km
- Integration of 64 dish MeerKAT to complete phase 1 array

SKA Low prototype

Space for SKA



SKA Mid prototype: Foundations

SKA Mid prototype: Panel molds

Picture: CETC54

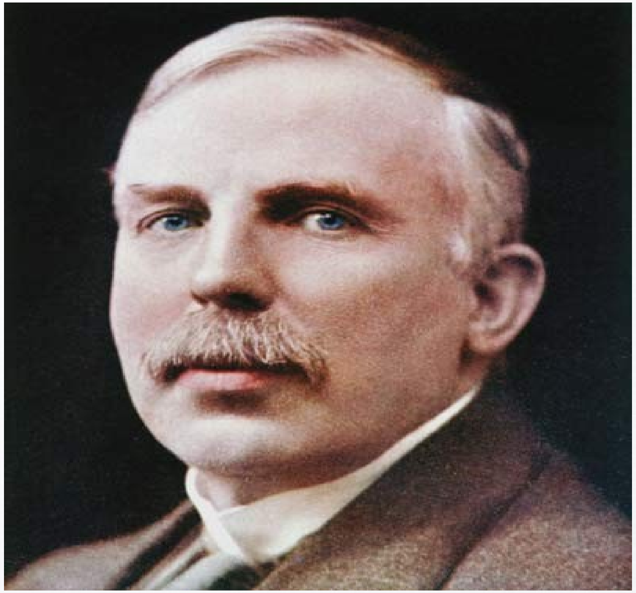
SKA Consortia

- Consortia are performing element designs
- SKAO is the central design authority
- For SKA 1:
  - Dish – The physical dishes, feeds and digitisation
  - SaDT – Signal and Data Transport (Included Synchronisation and Timing)
  - CSP – Central Signal Processing (Correlator, Beamformers and Non-imaging processing)
  - SDP – Science Data Processing
  - INFRA SA
  - INFRA AUS
  - LFAA – Low Frequency Aperture Array
  - TM – Telescope Manager
  - AIV – Assembly, Integration and Verification
- FOR the Advanced Instrumentation Program (SKA 2):
  - MFAA
  - WBSPF
  - PAF

SKA: What is next?

- “CDR Tomorrow”

- Now preparing for the element and system Critical Design Reviews
- Starting this year and extending through 2018
- Creation of a new Inter-governmental Organisation (IGO)
- Plan is to have agreements for the IGO in place this year
- Followed by ratification in each member country
- IGO comes into force early 2019
- Construction phase begins



From Alistair McPherson's presentation at the SKA Engineering Meeting 2017 (and 2016)

"Gentlemen, we have run out of money. It's time to start thinking."
— Ernest Rutherford

SKA1 construction *provisional* totals – Phil Diamond SKAO

Element	Estimate (M Euro incl. contingency) - Feb 2017	Estimate (M Euro incl. contingency) - Jun 2017	Change	% Change	Reason
AIV	32.8	34.3	1.6	5	Product Assurance and Admin functions increased per Cost Review
CSP	125.9	110.1	-15.8	-13	Frequency slice architecture for Mid.CBF adopted (ECP-170017 in transit)
DSH	173.7	173.2	-0.5	0	
INAU	96.0	[illegible]	[illegible]	[illegible]	[illegible]
INSA	67.9	[illegible]	[illegible]	[illegible]	[illegible]
LFAA	107.9	111.7	3.8	4	Shipping costs included per Cost Review
SaDT	66.7	57.1	-9.6	-14	Updated vendor quotes; some re-use of MeerKAT timescale; reduced component costs; refined software labour costs
SDP	114.5	114.5	0.0	0	
TM	43.7	43.0	-0.6	-1	
Totals	829.0	806.4	-22.6	-3	

€917M □ €806M

Updated CCP list (page 1/2)

WS / Origin	Description	LOW / MID / COMMON	Science Implication	Science Impact
5.39	INFRA_SA Renewable energy to outer dishes	MID	None	1
5.3	Maximise use of code produced during Pre-Construction	COMMON	None	1
5.38	Simplify DDBH LOW	LOW	None	1
5.38	Simplify DDBH MID	MID	None	1
5.25.2	Reduce PSS-MID: A, 750 nodes to 500 nodes	MID	Likely none, or small reduction of pulsar search parameter space.	1
5.25.2	Reduce PSS-LOW: A, 250 nodes to 167 nodes	LOW	Likely none, or small reduction of pulsar search parameter space.	1
5.35	Reduce CBF-MID: Freq. Slice variant of CSP design vs. MeerKAT-based design	MID	None	1
5.19	MID Frequency and Timing Standard: SaDT solution vs. MeerKAT-based solution	MID	None	1
5.36	MID SPF Digitisers: DSH solution vs. MeerKAT-based solution	MID	None	1
5.26 / 5.29	LOW RPF: Early Digital Beam Formation vs. Analogue Beam Formation	LOW	None	1
2	LOW Antenna: Log Periodic Design vs. Dipole Design	LOW	None of the current designs meet the L1 requirements	3
8	SDP- HPC: Deploy 200 Pflops (rather than 260 Pflops)	COMMON	Lower allowed duty cycle for HPC-intensive observations.	2
5.24.3	Reduce Bmax MID from 150 to 120 km: Case A, remove 3 dishes, but keep infra to 150km	MID	Reduction of maximum achievable resolution by 20%, although can be partially recovered with data weighting and longer integration times.	2
5.24.2	Reduce Bmax MID from 150 to 120 km: Case B, remove infra, but add dishes to core	MID	Reduction of maximum achievable resolution by 20%, although can be partially recovered with data weighting and longer integration times.	2
5.24.1	Reduce Bmax MID from 150 to 120 km: Case C, remove infra, remove dishes	MID	Reduction of maximum achievable resolution by 20%, although can be partially recovered with data weighting and longer integration times.	2
5.5.2	Reduce MID Band 5 feeds: A, from 130 to 67	MID	Placement to be determined based on full community consultation.	2
5.25.2	Reduce PSS-LOW: B, 167 nodes to 125 nodes	LOW	Likely reduction in processed PSS beam number (1.3x) or pulsar search parameter space	2
5.25.2	Reduce PSS-MID: B, 500 nodes to 375 nodes	MID	Likely reduction in processed PSS beam number (1.3x) or pulsar search parameter space	2

Updated CCP list (page 2/2)

8	SDP- HPC: Deploy 150 Pflops (from 200 Pflops)	COMMON	Lower allowed duty cycle for HPC-intensive observations.	3
5.30.0	Reduce Bmax LOW to 50km: A, remove infra, add 18 stations to core	LOW	Science Risk to EoR: Bmax.	3
5.30.0	Reduce Bmax LOW to 50km: B, remove 18 stations	LOW	Science Risk to EoR: Bmax	3
5.30a	Reduce Bmax LOW to 40km: C, remove next 18 stations	LOW	Science Risk to EoR: Bmax	3
8	SDP- HPC: Deploy 100 Pflops (from 150 Pflops)	COMMON	Lower allowed duty cycle for HPC-intensive observations.	4
8	SDP- HPC: Deploy 50 Pflops (from 100 Pflops)	COMMON	Lower allowed duty cycle for HPC-intensive observations.	4
5.31	Reduce CBF-LOW BW: A, 300 to 200 MHz	LOW	Longer observing times for continuum applications (1.5x)	4
5.25.2 / Deeper Savings	Reduce PSS-LOW: C, 125 nodes to 83 nodes	LOW	Likely reduction in processed PSS beam number (2x) or pulsar search parameter space	4
5.25.2 / Deeper Savings	Reduce PSS-MID: B, 375 nodes to 250 nodes	MID	Likely reduction in processed PSS beam number (2x) or pulsar search parameter space	4
5.13.2	Reduce Bandwidth output of band 5 to 2.5GHz	MID	Longer Band 5 observing times for some applications (2x)	4
5.35	Reduce MID CBF and DSH BW: 5 to 1.4 GHz	MID	Longer observing times to achieve continuum sensitivity in Band 5 (3.6x)	4
5.24 / Deeper Savings	Remove 11 MID Dishes from core	MID	10% Array sensitivity loss in core	4
5.30 / Deeper Savings	Remove 54 LOW stations from core	LOW	10% Array sensitivity loss in core	4
5.24 / Deeper Savings	Remove additional 11 MID Dishes from core	MID	20% Array sensitivity loss in core	4
5.30 / Deeper Savings	Remove additional 54 LOW stations from core	LOW	20% Array sensitivity loss in core	4
5.24.2	Reduce Bmax MID from 120 to 100 km: D, remove infra, remove next 3 dishes	MID	Lose Science (Planetary disks, High resolution Star Formation)	4
5.5.1	Remove MID Band 1 feeds: 105 to 0	MID	Lose Science (Cosmology, Galaxy Evolution)	4
5.5.2	Reduce MID Band 5 feeds: B, from 67 to 0	MID	Lose Science (Planetary disks, Star Formation)	4

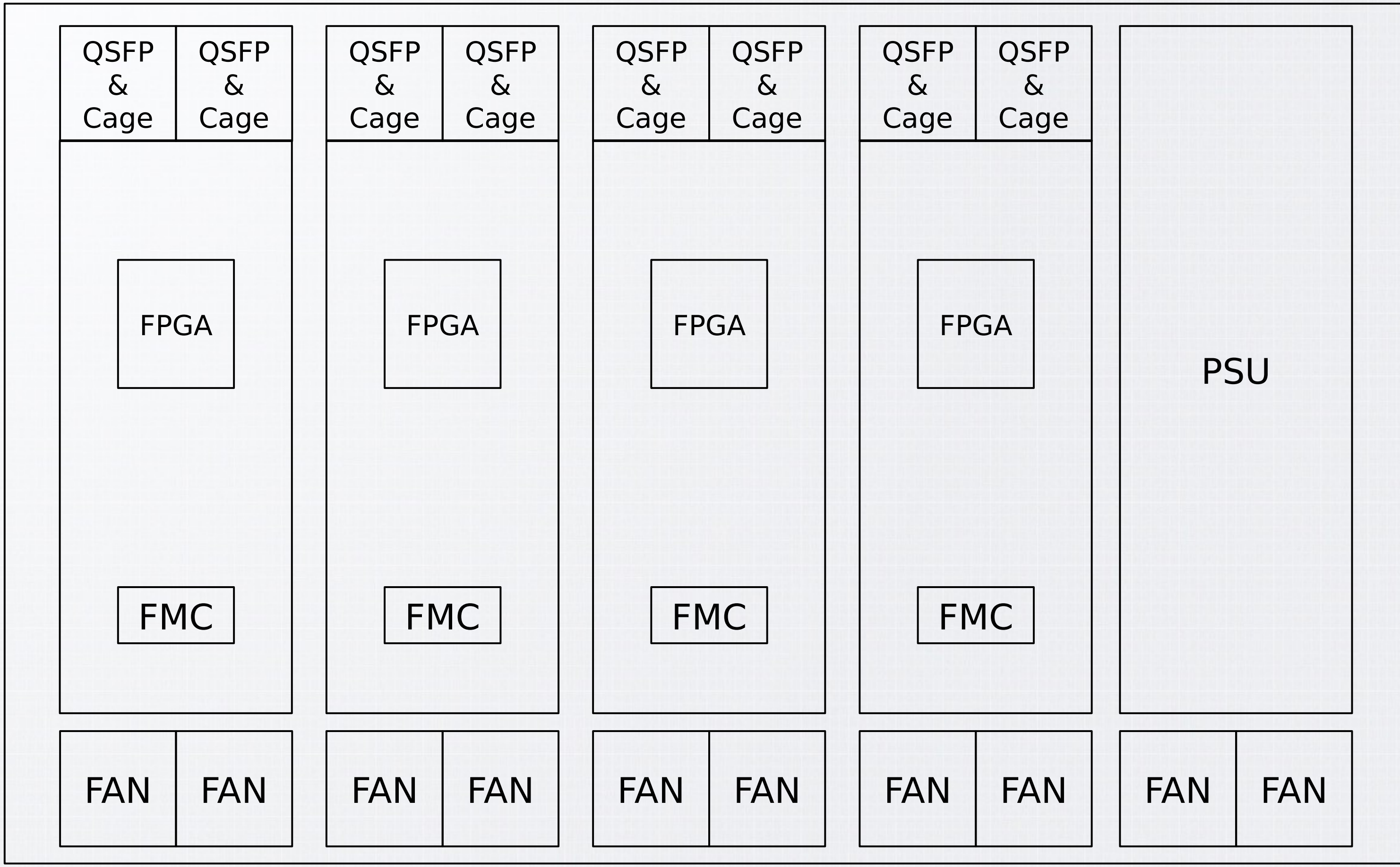
“DCE” ‘proposal’

- What would happen if we reused as much of MeerKAT as possible?
- Goal is to have no impact on science
- Only SKA1 Mid
- Allowed half of Euro 674 M cost cap
- Construction starts in 2019…
- … but we only need to deploy a large scale system by 2022
- SKARAB2 could be Virtex Ultrascale+ or Stratix 10 with HBM
- SKARAB2 is a risk mitigation for SKARAB3, which is the preferred family for SKA in ~2022 timeframe
- Increase density to 4 devices per 1U
- Power up to 130W per device, ~23kW per rack

A few key SKA CSP specifications

- Up to 5GHz instantaneous bandwidth (band 5)
- 130 15m antennas + 64 13.5m MeerKAT antennas
- Beamformers for:
  - VLBI – up to 4 beams with adjustable bandwidth
  - PSS – search. Up to 1500 beams at 300MHz bandwidth
  - PST – timing. 16 beams at full bandwidth
- Correlation
  - 64k channels WB
  - Zoom windows (4, 8, 16, 32, 64, 128, 256 MHz), 16k channels

SKARAB2 Block Diagram



SKARAB2 Hardware Proposal

- SKARAB vs SKARAB2

SKARAB	SKARAB2
Ethernet: 4 x 40GbE	Ethernet: 2 x 100GbE
Memory: 4GB HMC x 3	Memory: HBM
FPGA: 1 x Virtex 7	FPGA: 4 x Virtex UltraScale+
Dimensions: 1U	Dimensions: 1U
Power Consumption: 125W	Power Consumption: 684W
Cooling: Fan Air Flow	Cooling: Front to Back Fan Air Flow (TBD)

SKARAB vs SKARAB2 FPGA Specs

SKARAB Virtex 7 (XC7VX690T)

693120 Logic Cells

80 x SERDES

- 64 used for I/O mezzanine sites @ 10 Gbps
- 1 used for PCI-E to COM-E module site

1470 x 36Kb RAM Blocks (~52 Mb)

3600 DSP Slices

1927 pins
1000 single ended I/O

SKARAB 2 Virtex UltraScale (VU33P/VU35P)

962000-1907000 Logic Cells

32-64 x SERDES

- @ 32.75 Gbps

RAM Blocks (~23.6 - 47.3 Mb)

UltraRam (90-180 Mb)

HBM: 8GB

2880-5952 DSP Slices

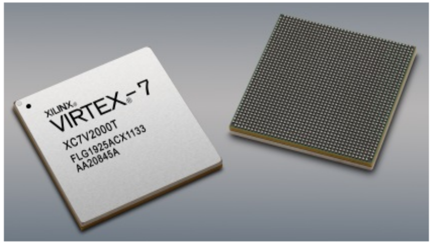
208 - 416 single ended I/O
2-5 x 100G Ethernet

SKARAB FPGA Specs in Detail

SKARAB Compute: Virtex 7 FPGA

peralex
the sense of signals

- 693120 Logic Cells
- 80 x SERDES
  - 64 used for I/O mezzanine sites @ 10 Gbps
  - 1 used for PCI-E to COM-E module site
- 1470 x 36Kb RAM Blocks (~52 Mb)
- 3600 DSP Slices
- 1927 pins



	Part Number	XC7VX690T
	EasyPath™ Cost Reduction Solutions[1]	XCE7VX690T
Logic Resources	Slices	108,300
	Logic Cells	693,120
	CLB Flip-Flops	866,400
Memory Resources	Maximum Distributed RAM (Kb)	10,888
	Block RAM/FIFO w/ ECC (36 Kb each)	1,470
	Total Block RAM (Kb)	52,920
Clocking	CMTs (1 MMCM + 1 PLL)	20
I/O Resources	Maximum Single-Ended I/O	1,000
	Maximum Differential I/O Pairs	480
Integrated IP Resources	DSP Slices	3,600
	PCIe® Gen2[2]	–
	PCIe Gen3	3
	Analog Mixed Signal (AMS) / XADC	1
	Configuration AES / HMAC Blocks	1
	GTX Transceivers (12.5 Gb/s Max Rate)[3]	–
	GTH Transceivers (13.1 Gb/s Max Rate)[4]	80
	GTZ Transceivers (28.05 Gb/s Max Rate)	–
Speed Grades	Commercial	-1, -2
	Extended[5]	-2L, -3
	Industrial	-1, -2

	Package[6]	Dimensions (mm)	GTH)
	FFG1157 / FFV1157[7]	35 x 35	0, 600 (0, 20)
Footprint Compatible	FFG1761 / FFV1761[7]	42.5 x 42.5	0, 850 (0, 36)
	FHG1761	45 x 45	
	FLG1925	45 x 45	
	FFG1158 / FFV1158[7]	35 x 35	0, 350 (0, 48)
Footprint Compatible	FFG1926	45 x 45	0, 720 (0, 64)
	FLG1926	45 x 45	
	FFG1927 / FFV1927[7]	45 x 45	0, 600 (0, 80)
Footprint Compatible	FFG1928	45 x 45	
	FLG1928	45 x 45	
Footprint Compatible	FFG1930	45 x 45	0, 1000 (0, 24)
	FLG1930	45 x 45	

SKARAB2 FPGA Specs in Detail

<u>SKARAB 2 Virtex UltraScale (VU33P/VU35P – package compatible)</u>

- 962000-1907000 Logic Cells
- 32-64 x SERDES
  - @ 32.75 Gbps
- RAM Blocks (~23.6 - 47.3 Mb)
- UltraRam (90-180Mb)
- HBM: 8GB
- 2880-5952 DSP Slices
- 208 - 416 single ended I/O
- 2-5 x 100G Ethernet

Virtex® UltraScale+™ FPGAs

Device Name	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU31P	VU33P	VU35P	VU37P
System Logic Cells (K)	862	1,314	1,724	2,586	2,835	3,780	962	962	1,907	2,852
CLB Flip-Flops (K)	788	1,201	1,576	2,364	2,592	3,456	879	879	1,743	2,607
CLB LUTs (K)	394	601	788	1,182	1,296	1,728	440	440	872	1,304
Max. Distributed RAM (Mb)	12.0	18.3	24.1	36.1	36.2	48.3	12.5	12.5	24.6	36.7
Total Block RAM (Mb)	25.3	36.0	50.6	75.9	70.9	94.5	23.6	23.6	47.3	70.9
UltraRAM (Mb)	90.0	132.2	180.0	270.0	270.0	360.0	90.0	90.0	180.0	270.0
HBM DRAM (GB)	–	–	–	–	–	–	4	8	8	8
HBM AXI Interfaces	–	–	–	–	–	–	32	32	32	32
Clock Mgmt Tiles (CMTs)	10	20	20	30	12	16	4	4	8	12
DSP Slices	2,280	3,474	4,560	6,840	9,216	12,288	2,880	2,880	5,952	9,024
Peak INT8 DSP (TOP/s)	7.1	10.8	14.2	21.3	28.7	38.3	8.9	8.9	18.6	28.1
PCIe® Gen3 x16 / Gen4 x8	2	4	4	6	3	4	4	4	5	6
CCIX Ports[1]	–	–	–	–	–	–	4	4	4	4
150G Interlaken	3	4	6	9	6	8	0	0	2	4
100G Ethernet w/ RS-FEC	3	4	6	9	9	12	2	2	5	8
Max. Single-Ended HP I/Os	520	832	832	832	624	832	208	208	416	624
GTY 32.75Gb/s Transceivers	40	80	80	120	96	128	32	32	64	96
Extended[2]	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3
Industrial	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	–	–	–	–

Footprint compatible with 20nm UltraScale Devices with same footprint identifier

Footprint[3,4]	Dimensions (mm)	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU31P	VU33P	VU35P	VU37P
		HP I/O, GTY 32.75Gb/s									
C1517	40x40	520, 40									
F1924[5]	45x45					624, 64					
A2104	47.5x47.5		832, 52	832, 52	832, 52						
	52.5x52.5[6]						832, 52				
B2104	47.5x47.5		702, 76	702, 76	702, 76	572, 76					
	52.5x52.5[6]						702, 76				
C2104	47.5x47.5		416, 80	416, 80	416, 104	416, 96					
	52.5x52.5[6]						416, 104				
D2104	47.5x47.5				676, 76	572, 76					
	52.5x52.5[6]						676, 76				
A2577	52.5x52.5				448, 120	448, 96	448, 128				
H1924	45x45							208, 32			
H2104	47.5x47.5								208, 32	416, 64	
H2892	55x55									416, 64	624, 96

SKA South Africa, a Business Unit of the National Research Foundation, is supervising South Africa's involvement in the SKA on behalf of the Department of Science & Technology.

Thanks