

Real-Time Resampling Processor for SWARM

Mark Peryer

Harvard Smithsonian Center for Astrophysics

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Presentation Overview

Background

Objectives

Design

Results

Future work

Background

Event Horizon Telescope (EHT)

Image the event horizon of SgrA*

Global network of telescopes

Very Long Baseline Interferometry (VLBI)



Submillimeter Array

Mauna Kea, Hawaii

8 element interferometer

32 GHz instantaneous bandwidth



SWARM

ROACH2 platform

ADCs record data at **4.576 GSps**

One Quadrant = **~38 Gigabits** every second!



Compatibility Issue

SMA

4.576 GHz

Frequency Domain



EHT

4.096 GHz

Time Domain

APHIDS

Non-real-time GPU resampling system



Improvements

APHIDS

X Costly

X Time Inefficient

X Quantization Error

Real-Time Resampler

✓ Inexpensive

✓ Instantaneous Results

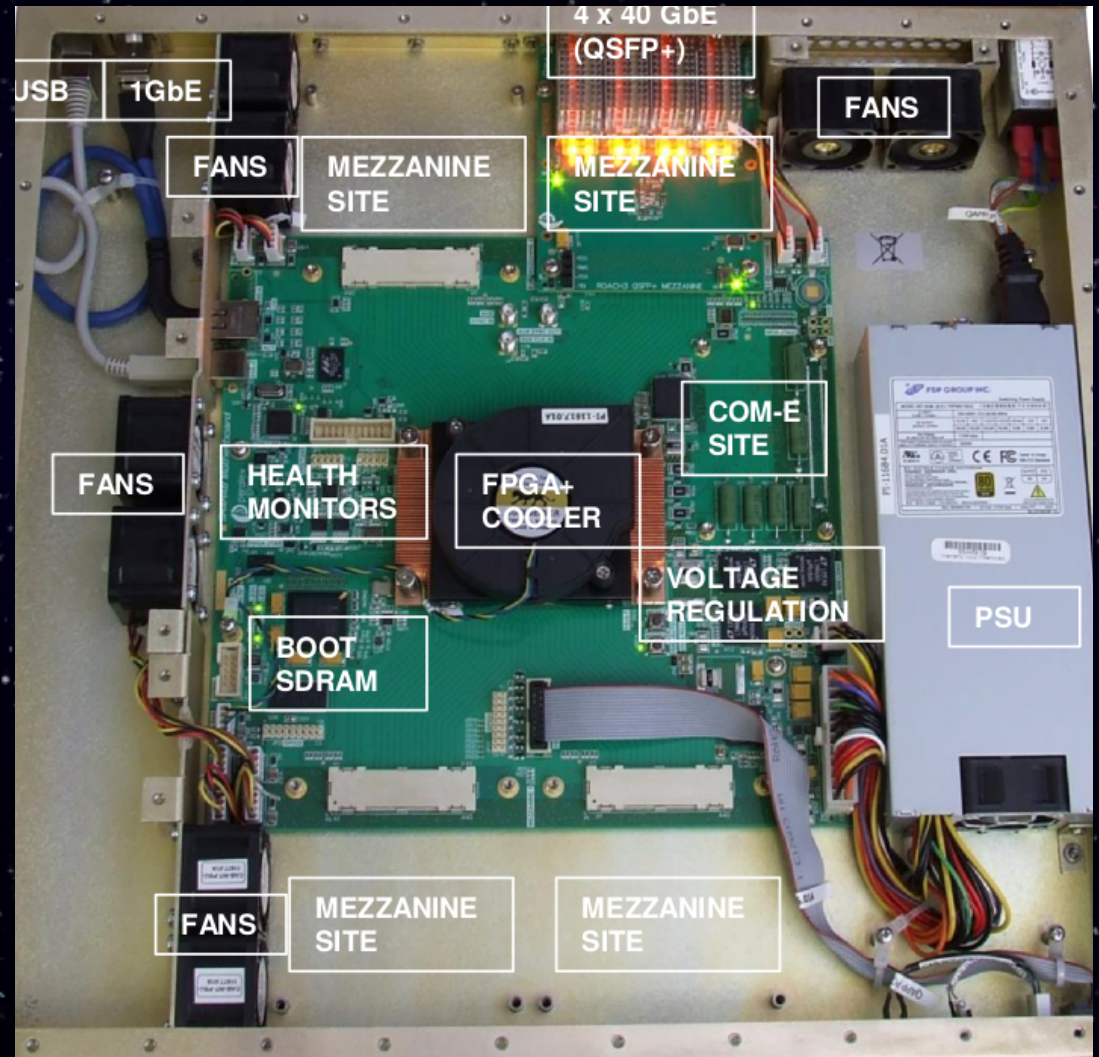
✓ Limited Quantization Error

Target Hardware

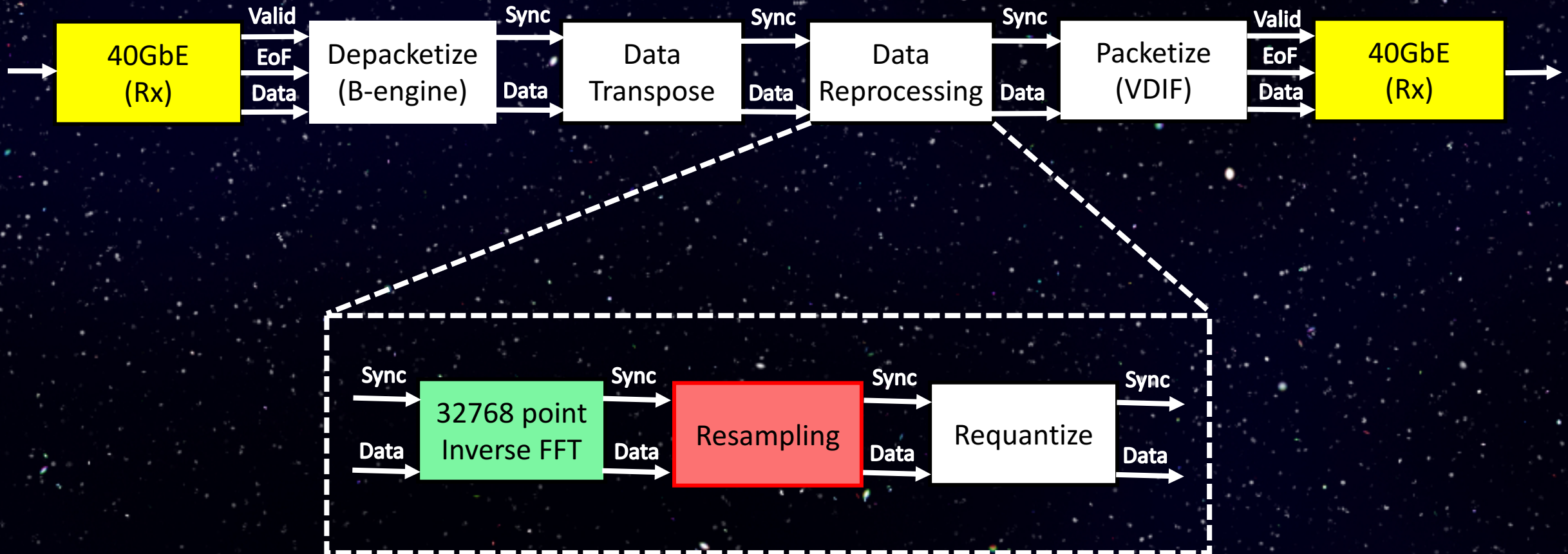
SKARAB

Virtex 7 FPGA

40 GbE interface



High-Level Overview

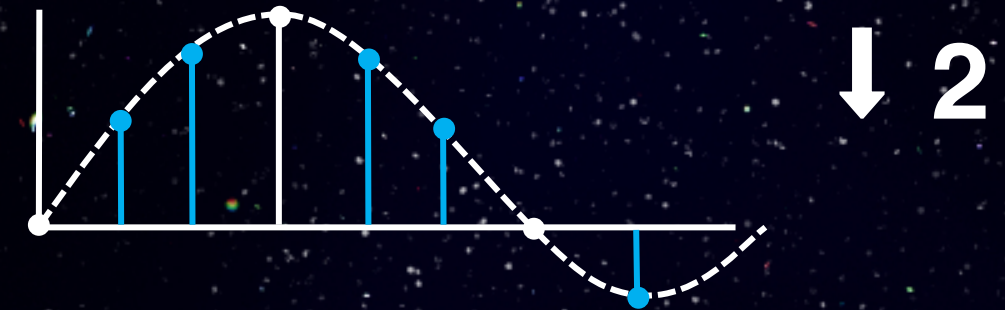
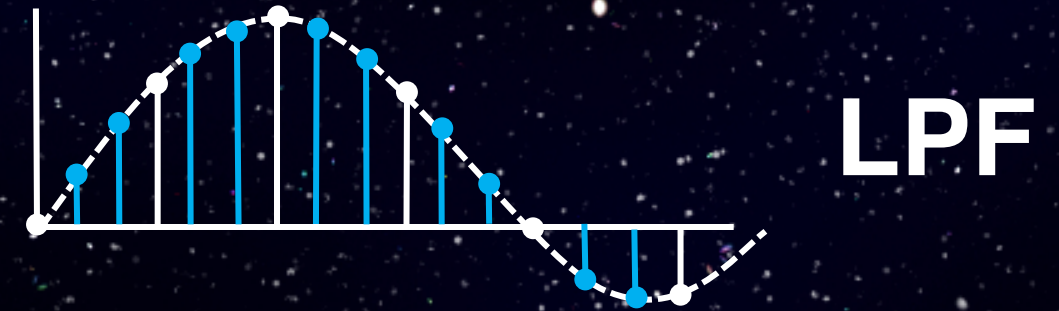
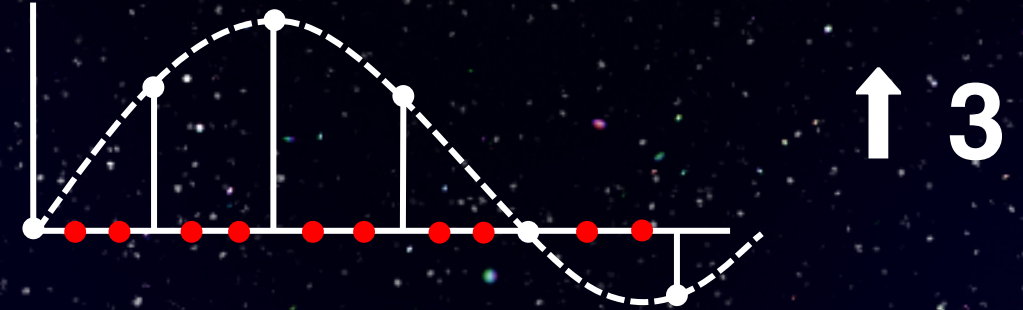
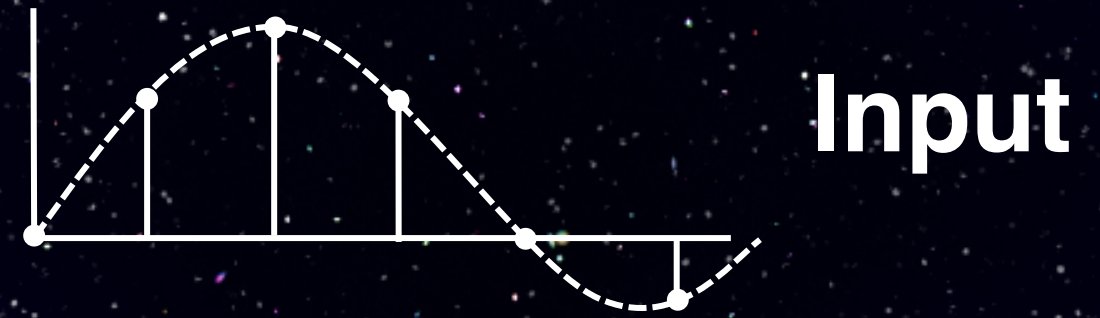
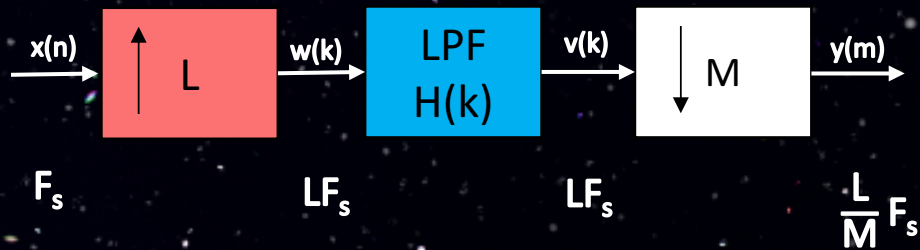


Resampling

$$\frac{4576}{4096} = \frac{143}{128}$$

Upsample by 128

Downsample by 143



Practicality

↑128 ↓143

585 billion samples every second!

Throw away 581 billion samples

Solution

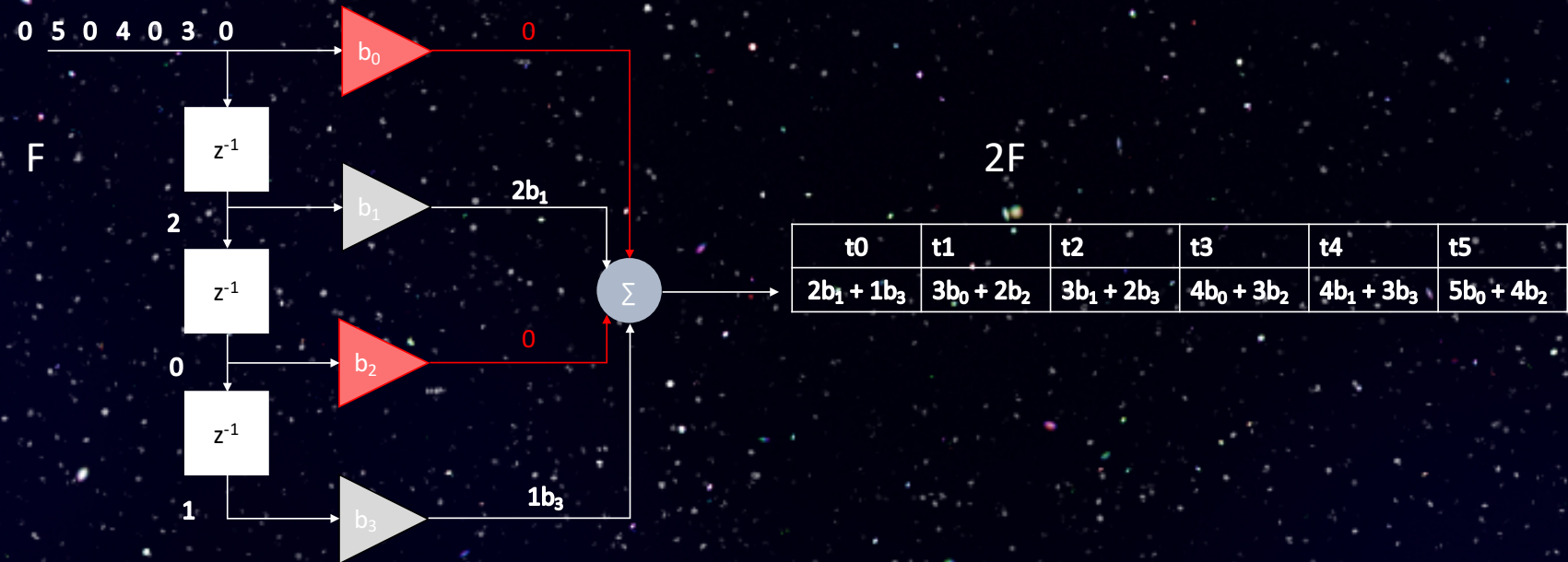
↑16 ↓17.875



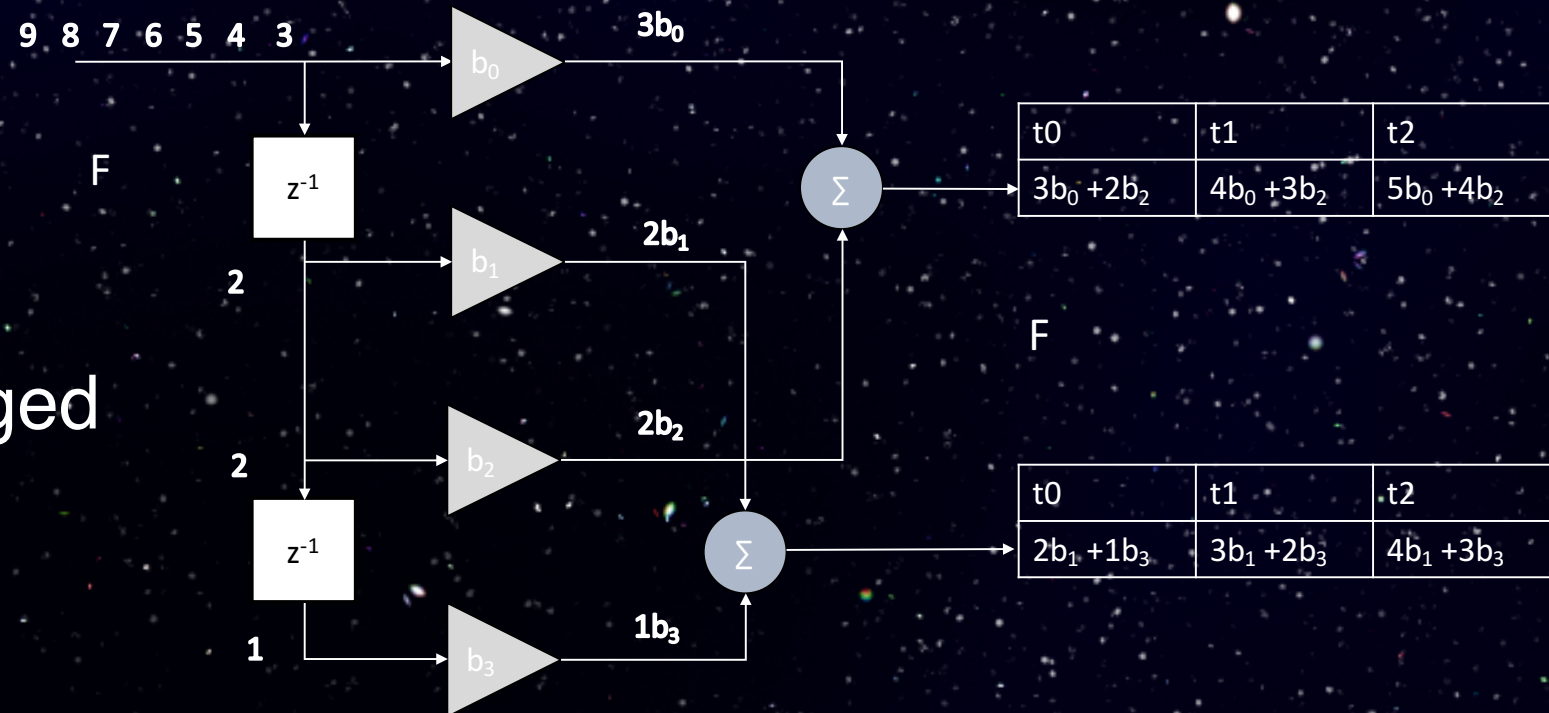
$$\frac{4576}{4096} = \frac{16}{143/8} = \frac{16}{17.875}$$

Upsampling

Inefficient
Clock rate increased



Efficient
Clock rate unchanged

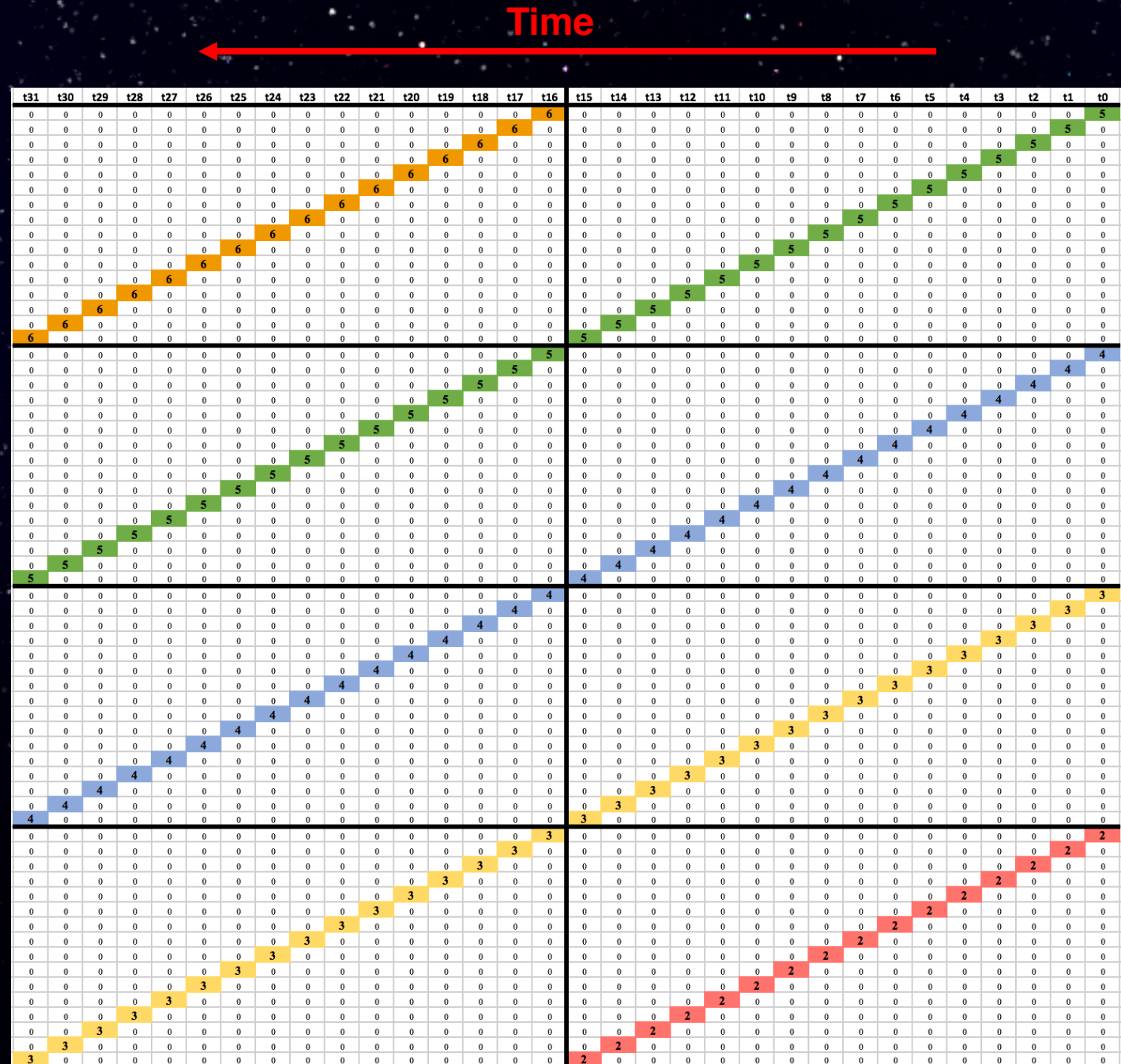


Scaling Up

4 samples every clock cycle

1 new sample every 16 clocks

Pattern repeats for parallel inputs



Hi_25_505
From
Workspace2

In

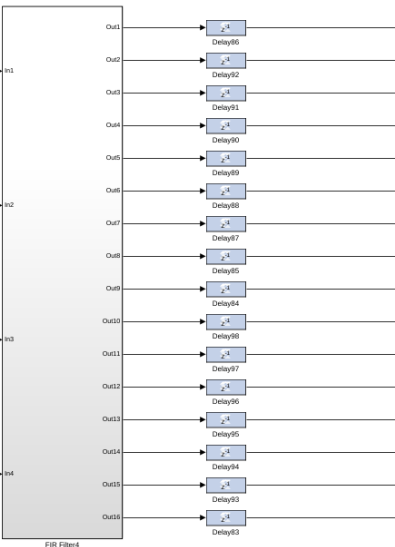
Gateway 142

Hi_25_505

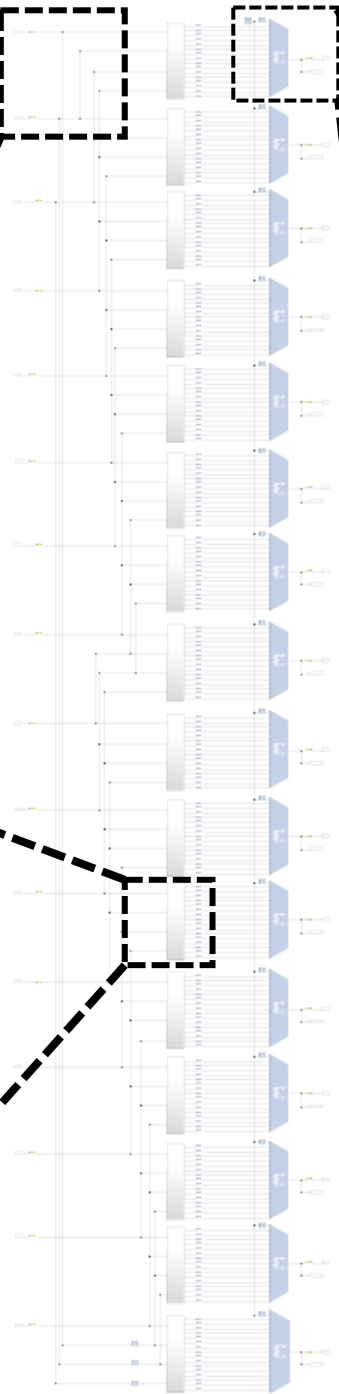
From
Workspace2

In

Gateway 142



FIR Filter4



Counter



ROM

sel

d0

d1

d2

d3

d4

d5

d6

d7

d8

d9

d10

d11

d12

d13

d14

d15

Mux15

z⁻¹

Out

Gateway Out15

output_mux1

To Workspace16

[mux16]

Goto15

FIR Filter

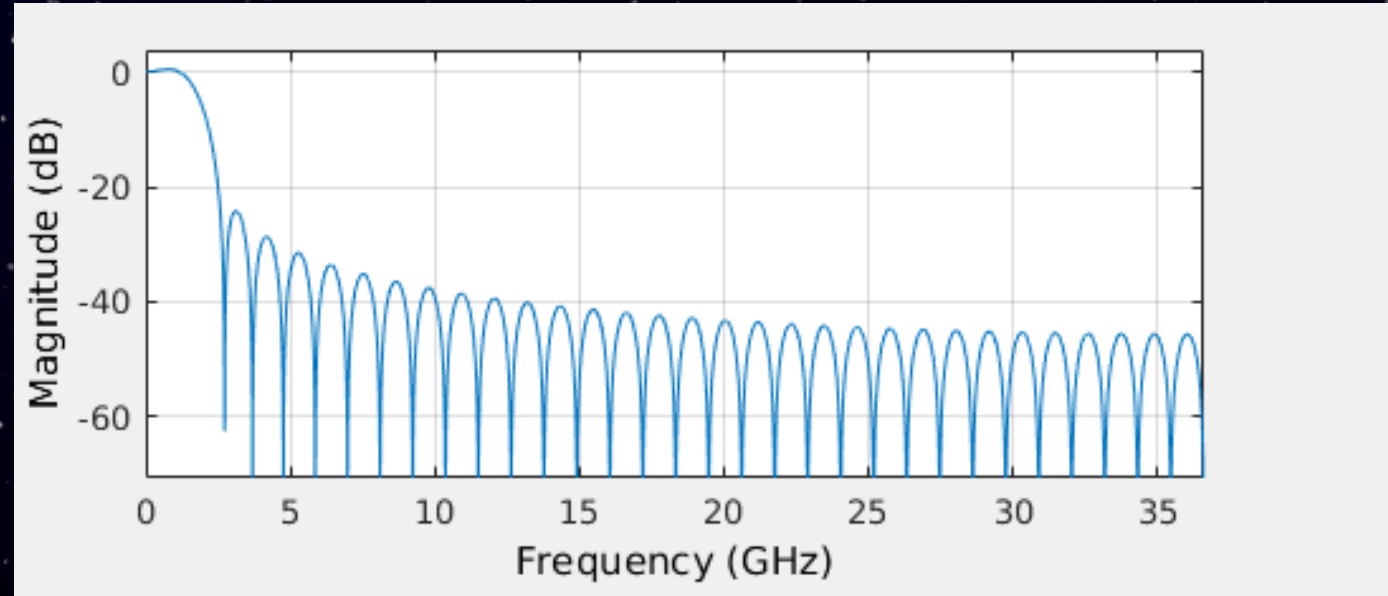
63rd order FIR filter

Low pass filter

64 coefficients

Least-squares linear phase

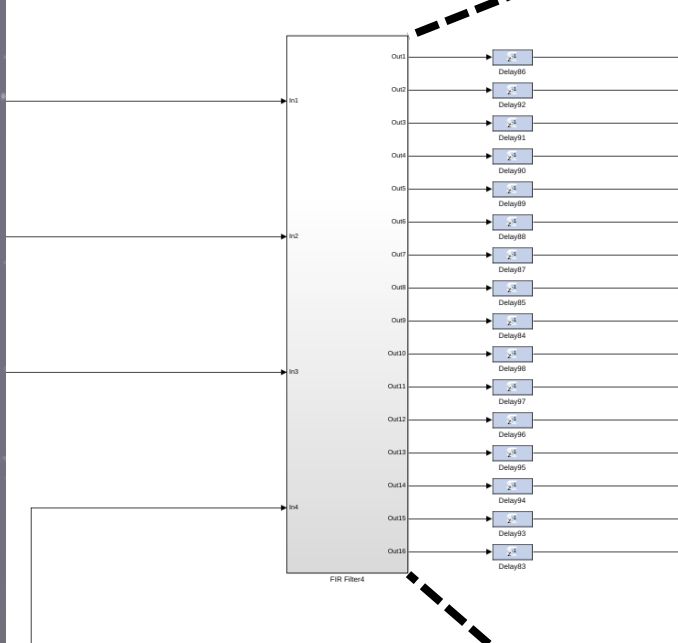
Magnitude response of filter



$$F_{\text{pass}} = 2.138 \text{ GHz}$$

$$F_{\text{stop}} = 2.288 \text{ GHz}$$

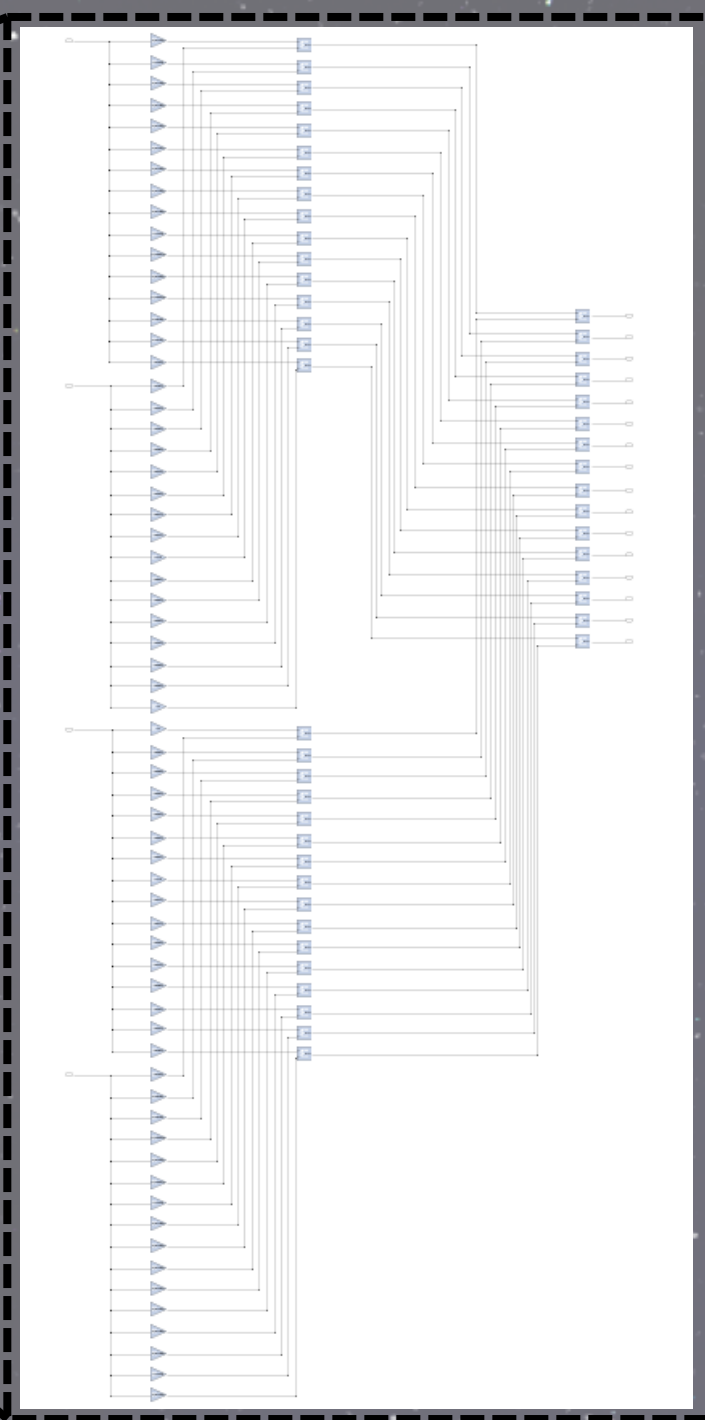
FIR Filter Design



16 Filters

1024 multiplies

768 adds



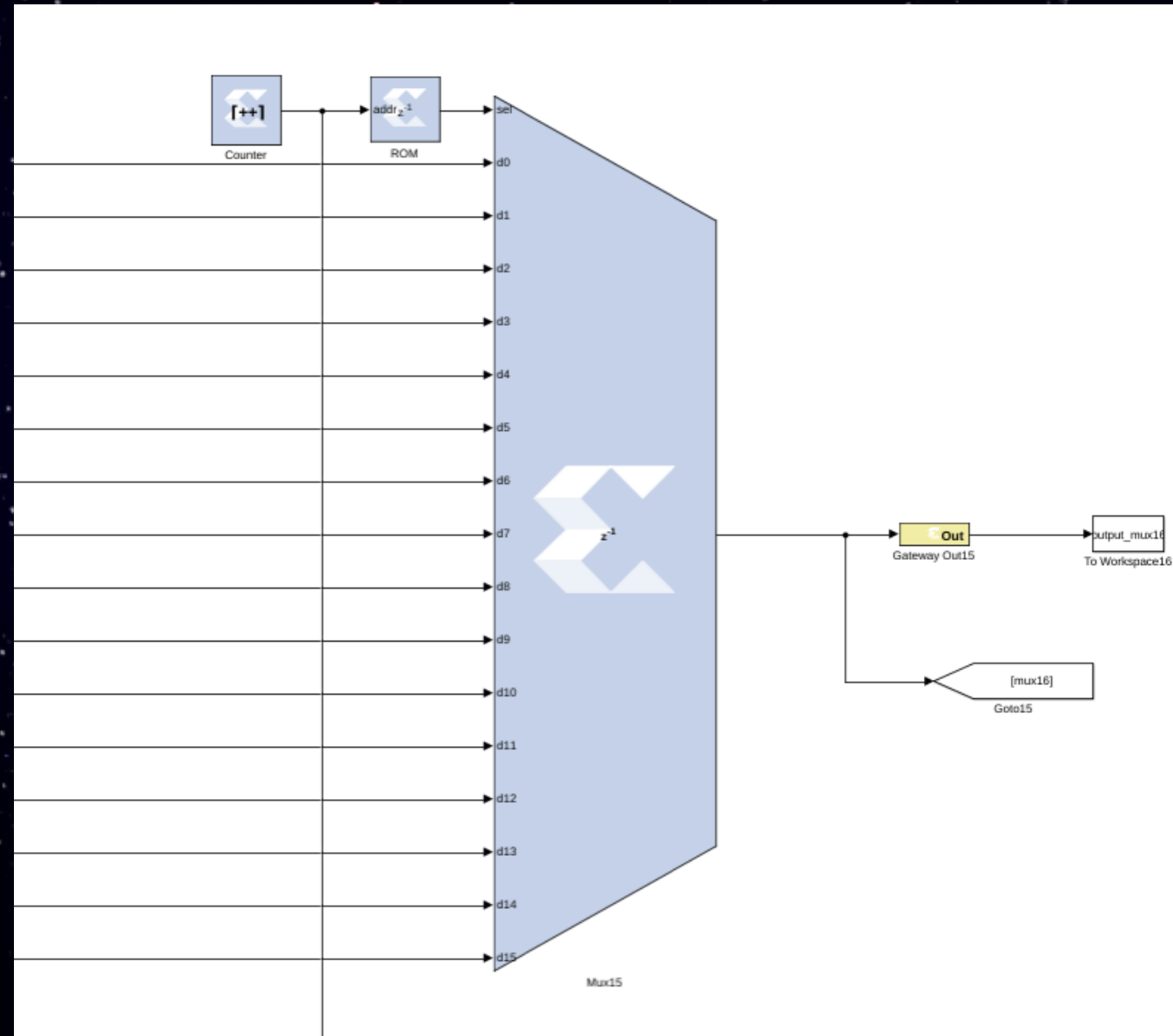
Downsampling

16 outputs every clock

↓ by 17 and 18

ROM stores mux select

Repeats every 143 clocks

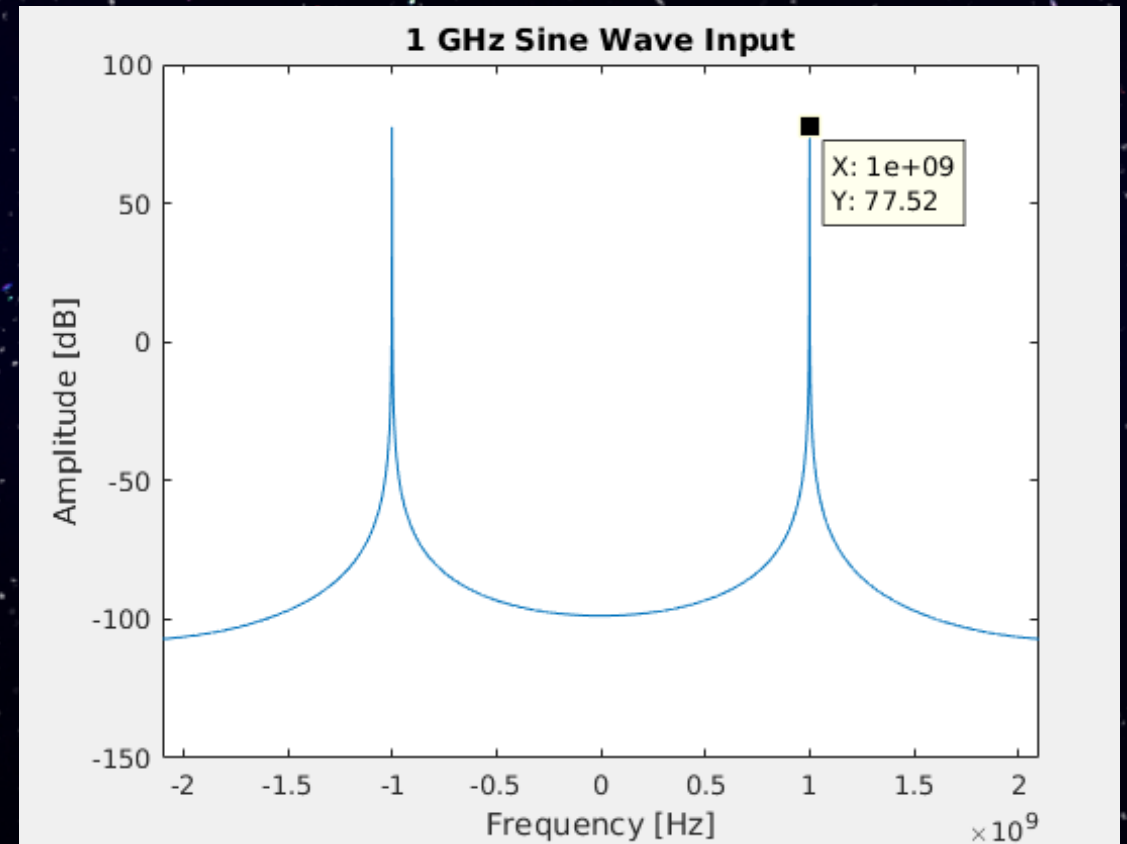


Simulated Input

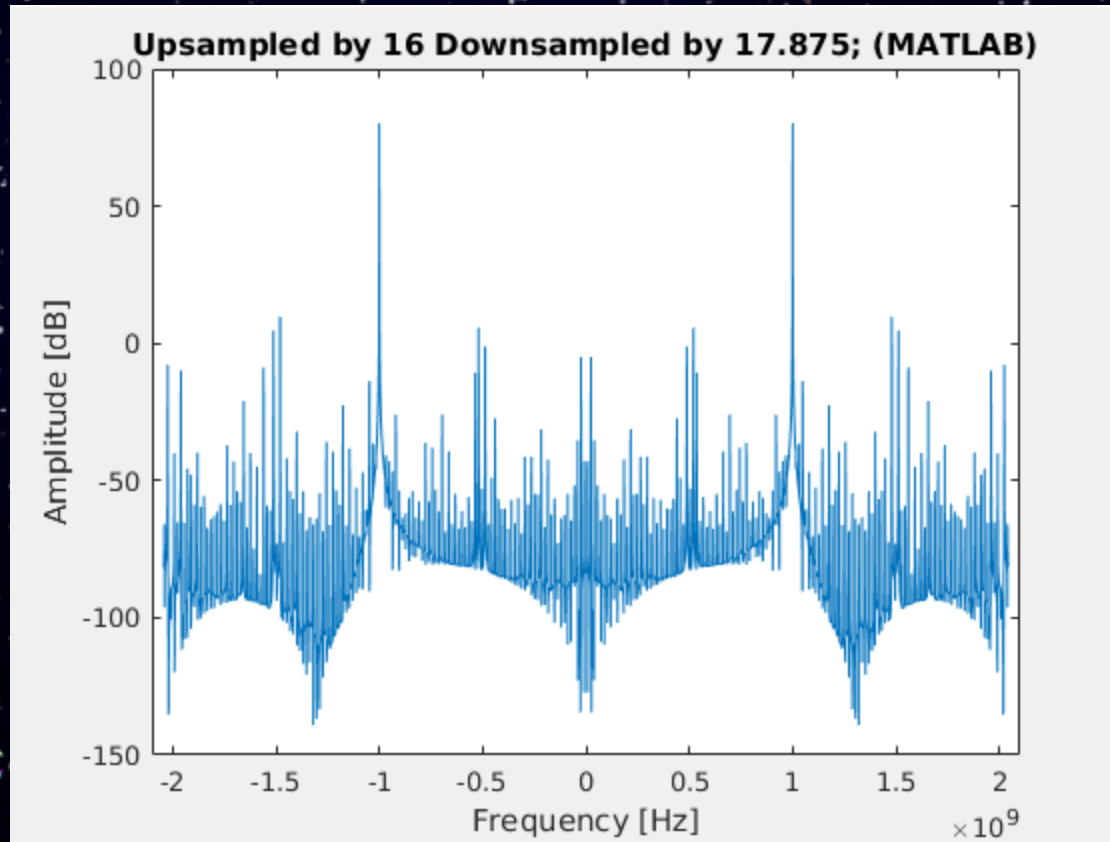
1 GHz sine wave

4.576 GHz sample rate

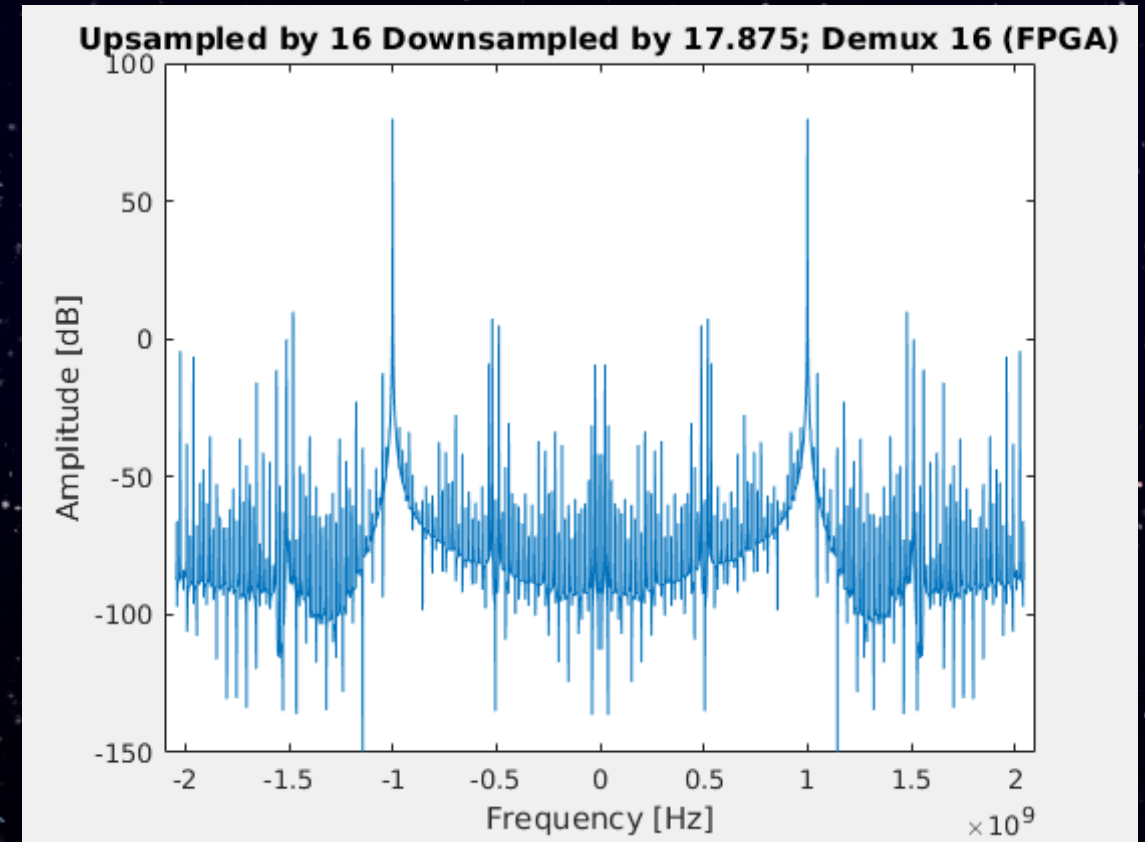
16 parallel samples per clock



Simulated Results



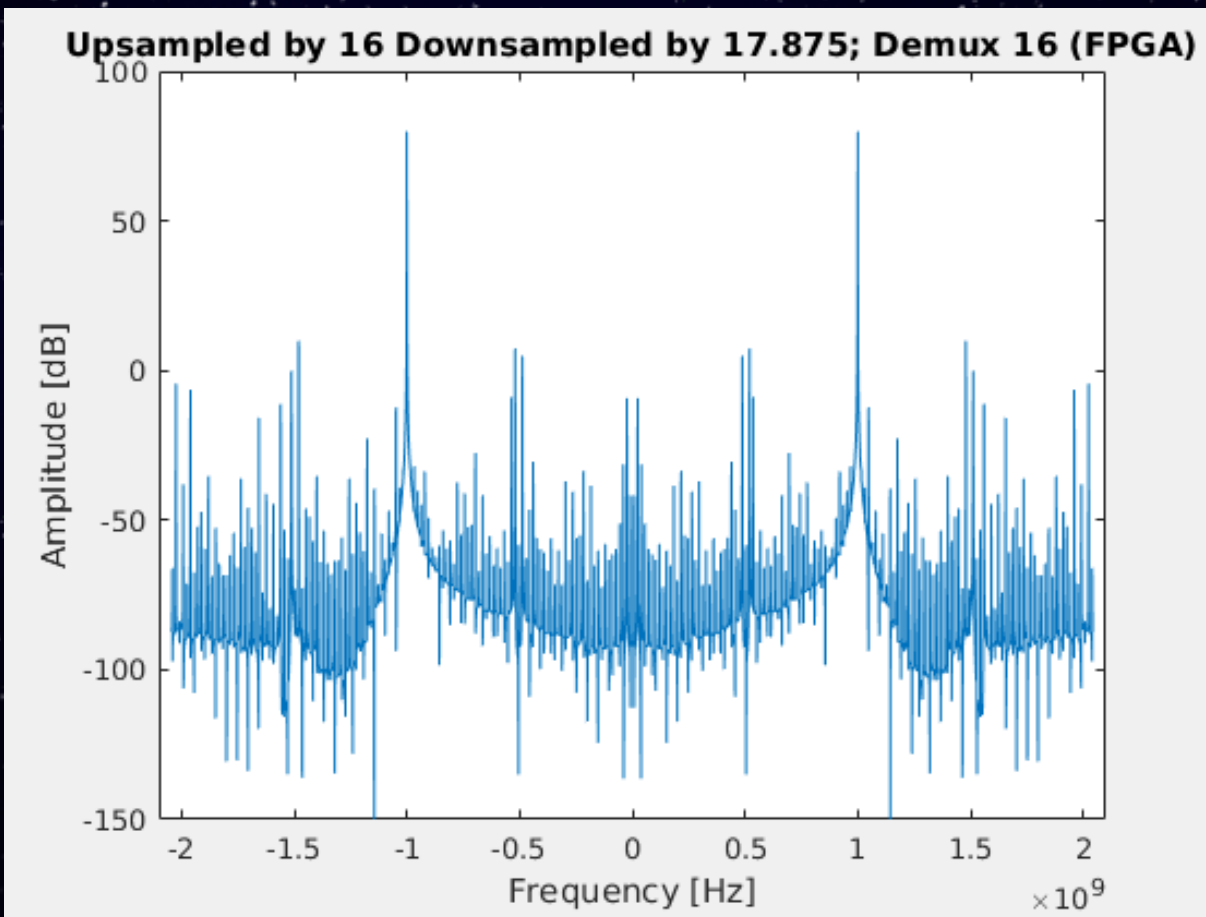
Theoretical output from MATLAB



Output from Simulink Design

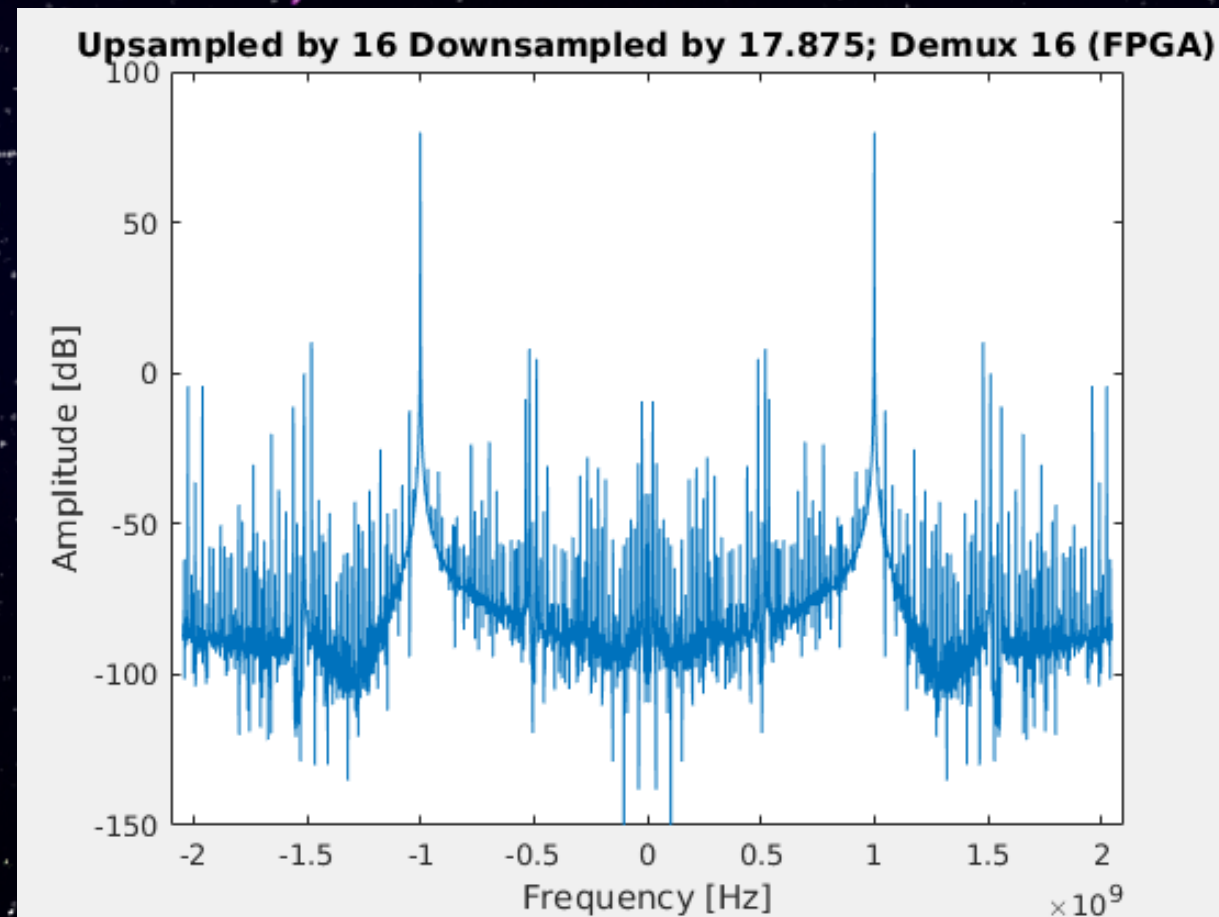
Bit Growth

Full bit depth



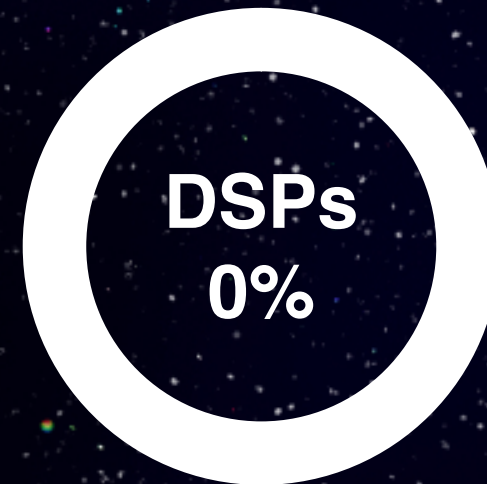
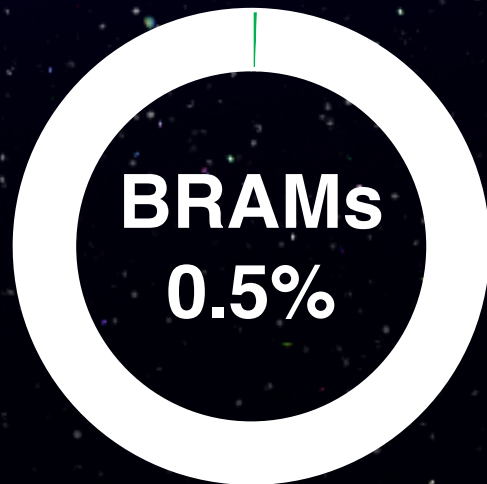
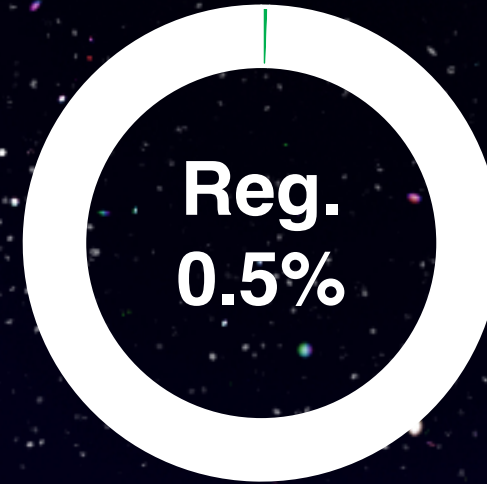
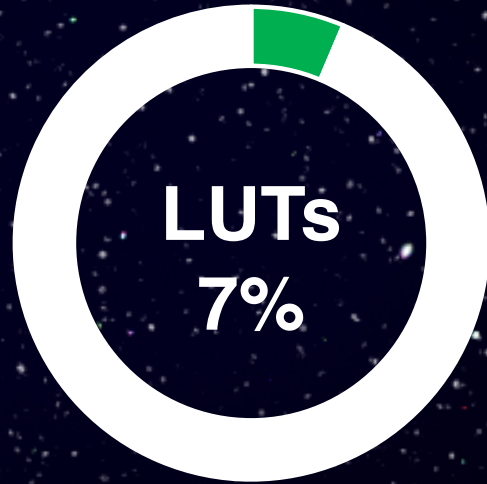
16_14 bit input
16_14 bit coefficients
34_28 bit output

Reduced bit depth



8_7 bit input
8_7 bit coefficients
18_14 bit output

Resource usage



Conclusion

Real Time Implementation

Parallel FIR Filter Design

Fits on Target Hardware

Future Work

Remove invalid outputs

Incorporate into Real-Time Resampling System

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Thank You

Questions?