RFI MITIGATING RECEIVER BACK-END FOR RADIOMETERS

Phaneendra Bikkina[1], Qingjun Fan[2], Wenlan Wu[1], Jinghong Chen[2] and Esko Mikkola[1]

[1] Alphacore, Inc., [2] University of Houston

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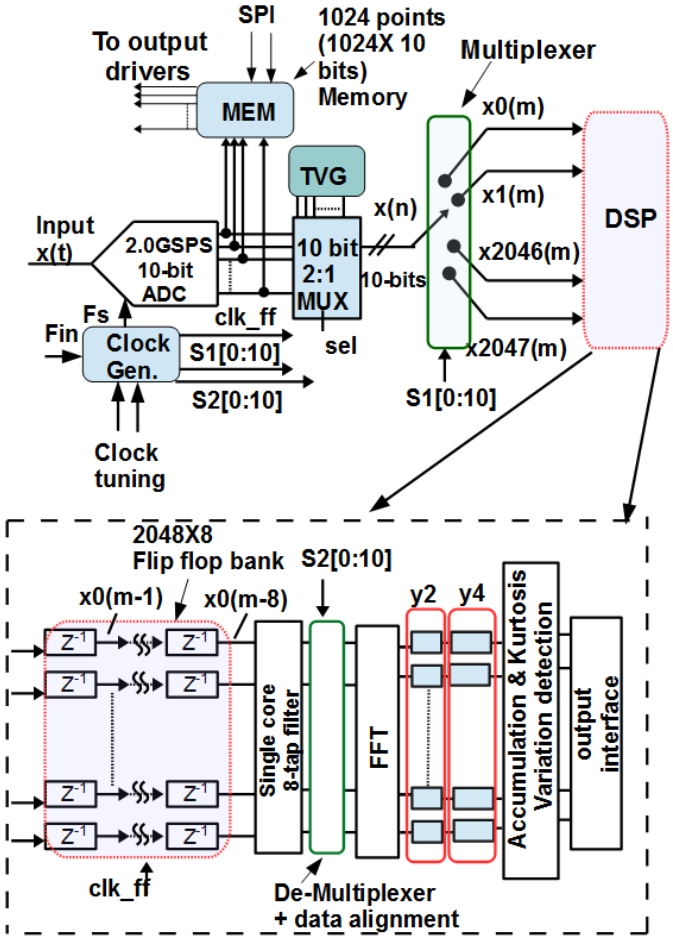
Introduction and Background

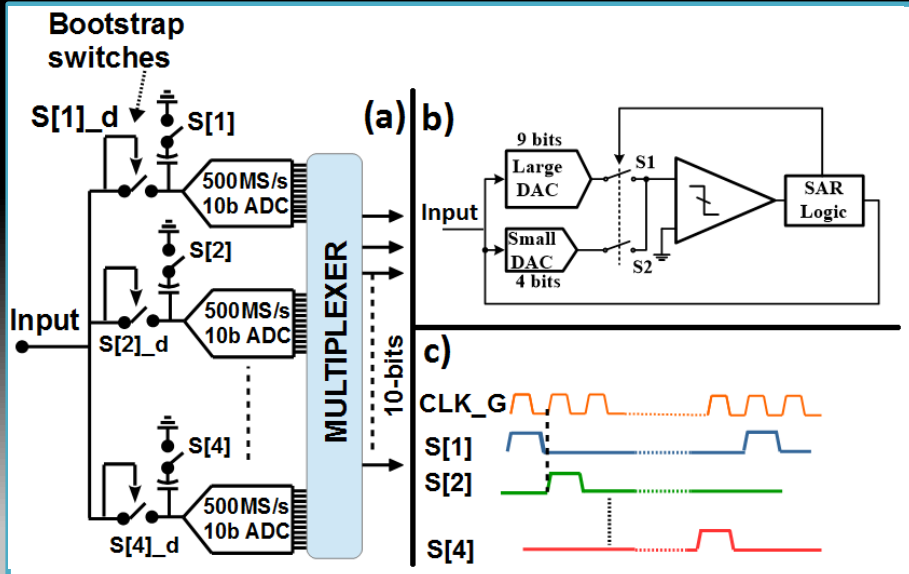
- The work presented here is part of a joint effort between Alphacore, Inc, University of Houston and NASA Jet Propulsion Lab (JPL) to develop a low-power, radiation-hard RFI mitigating receiver back-end for radiometers that can process over a gigahertz of signal bandwidth.
- The results of this work also enable applications that require low-power receivers that incorporate ADCs and back-end filters, without the need for RFI mitigation, e.g., spectrometers used in MKID arrays.
- Other similar systems that we are aware of are 'Mars Spec' and Single-chip Planetary Low-power ASIC Spectrometer with High-resolution (SPLASH) ASIC.
  - 'Mars Spec' is a DSP-only solution, comprised of an off-chip 1.5 GS/s ADC with 4096 channels while consuming 2.7W.
  - SPLASH has an 3GS/s ADC, 8000-channel FFT consuming 950mW.

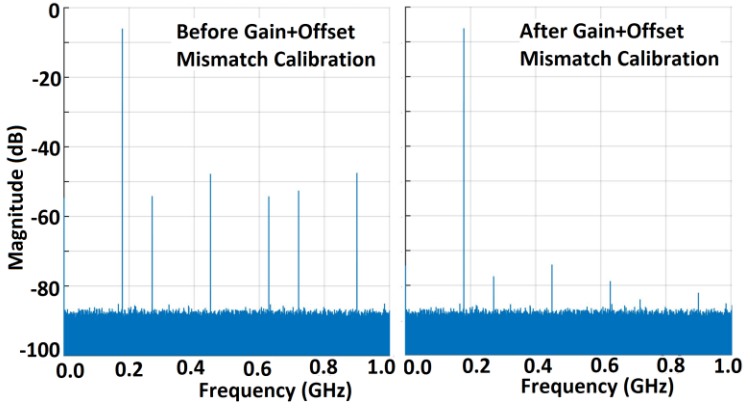
RFI Mitigating Receiver Back-End



- 3.2GS/s 12-bit ADC (analog front end)
- ADC sampling rate can be adjusted with clock tuning using clock generator block
- 1024 sub-band low power polyphase filters
- Kurtosis for RFI detection and mitigation
- on-chip memory for calibration/characterization of the ADC
- Total power of ADC 35.7mW for >9bits ENOB and 12.7mW for >8bits ENOB

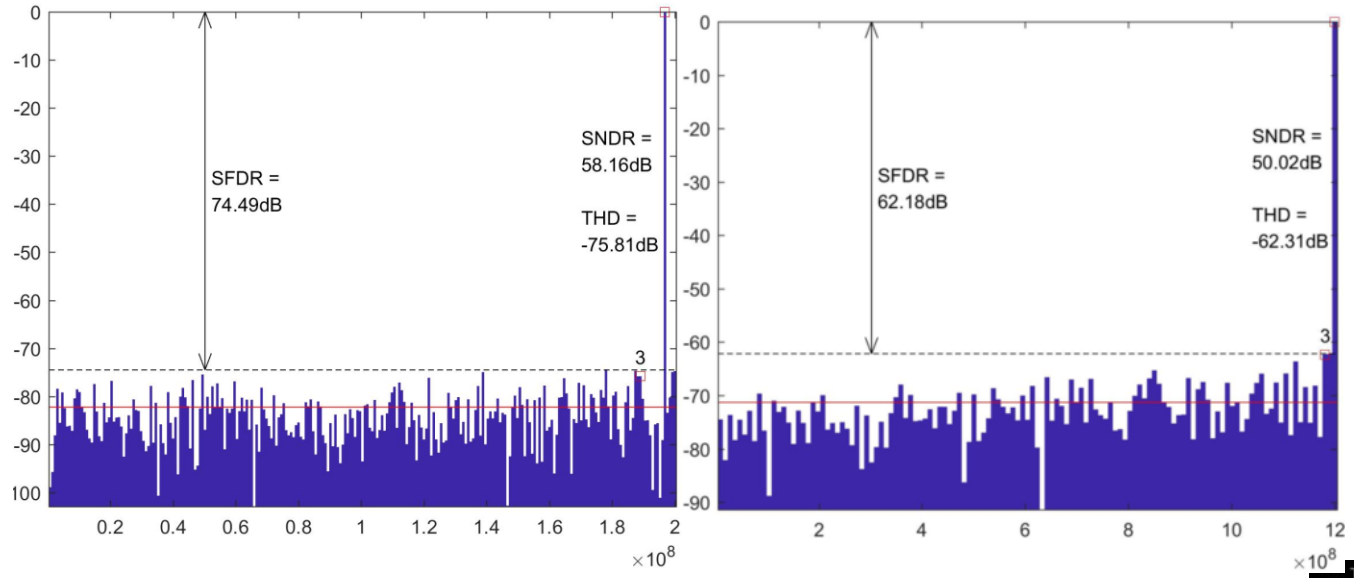
10-bit Time-Interleaved SAR (Successive Approximation Register) ADC



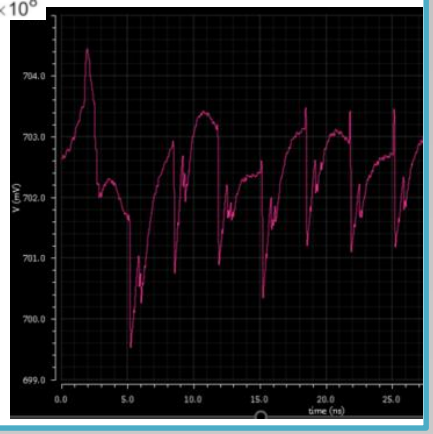


- 4-way time interleaved topology with high-bandwidth (5GHz input bandwidth) front-end sampling circuit
- Each SAR ADC channel uses a dual-DAC topology relaxing DAC settling time constraint for first few bits
- Over-ranging for calibration
- Does not require high frequency clock for sampling
- Gain mismatch is calibrated digitally using channels match expression for m^{th} channel as Gm = sqrt(($\Sigma y^2 m[n]$)/K) where K is the total number of channels and n varies from 1 to K
- Time skew calibration is mitigated by employing special skew control and pulse width control circuits
- Modified to 8–way interleaved due to layout performance degradation of sampling rate
- Higher sampling rate in each channel also requires high power consuming reference drivers (due to kickback noise on references)
- 8-channel 10-bit 2-3 GS/s tapeout scheduled for November 2017

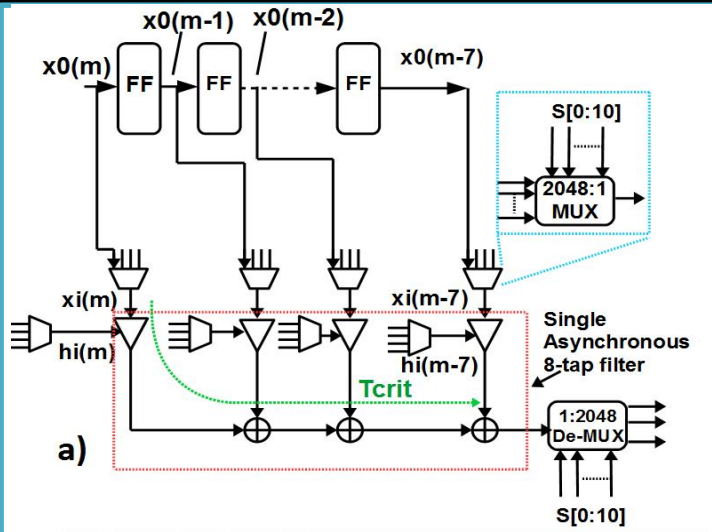
Parasitic extracted simulation results of ADC

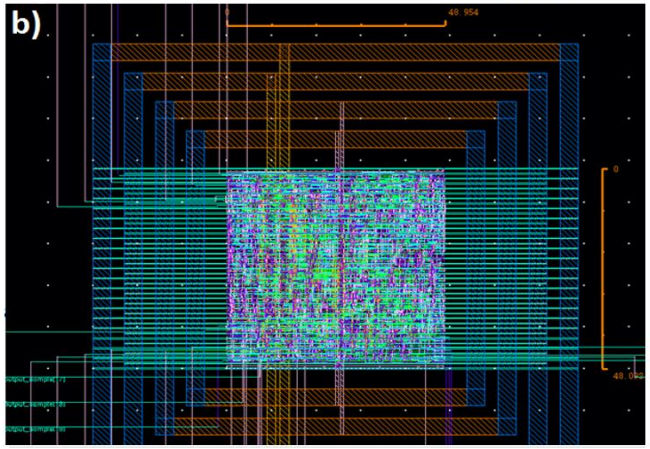


- Single channel post layout simulations shows 9.36 bits ENOB
- 8-channel time-interleaved has 8.1bits ENOB (program goal)
- Higher ENOB with channel randomization
- ENOB limited by reference voltage noise
- Power α reference voltage accuracy (reference buffer driver will have lower impedance)



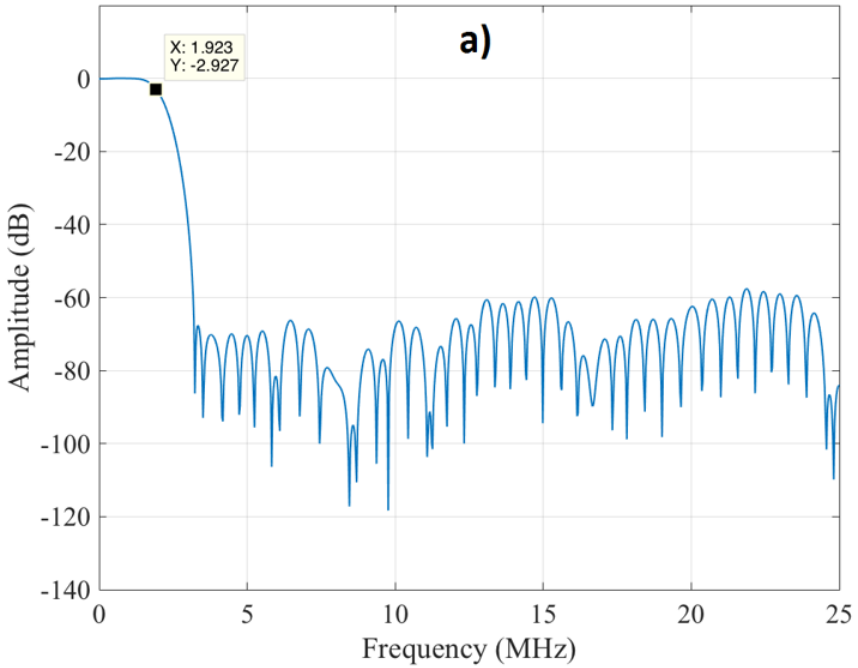
Polyphase Filter Bank's (PFB) Single core 8-tap filter with 10-bit input lines and 10-bit coefficients (1/2)

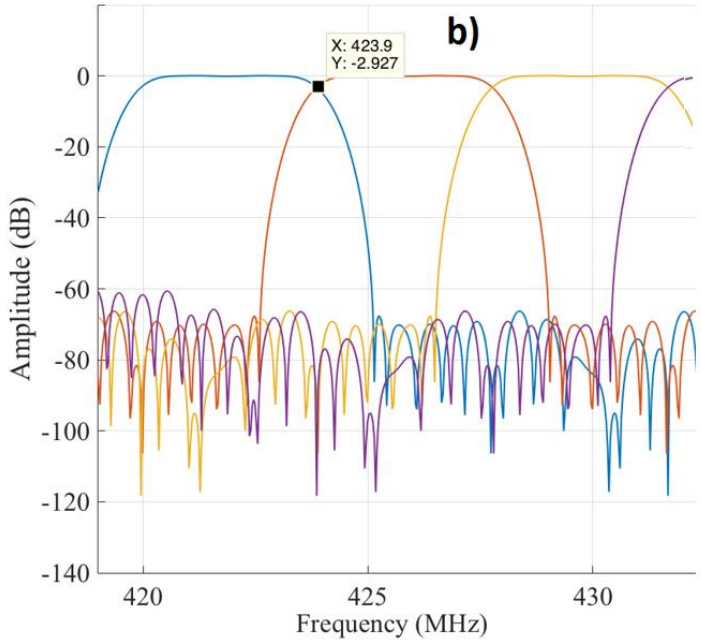




- 1024 sub-band PFB with maximum data throughput of 3GS/s and total area 0.0097mm^2
- Asynchronous single-core filter that works at very high data rate
- 11-bit switching bus (S[0:10]) synchronous to ADC's sampling clock
- Output is de-multiplexed to 2048 points (for 1024 point FFT)

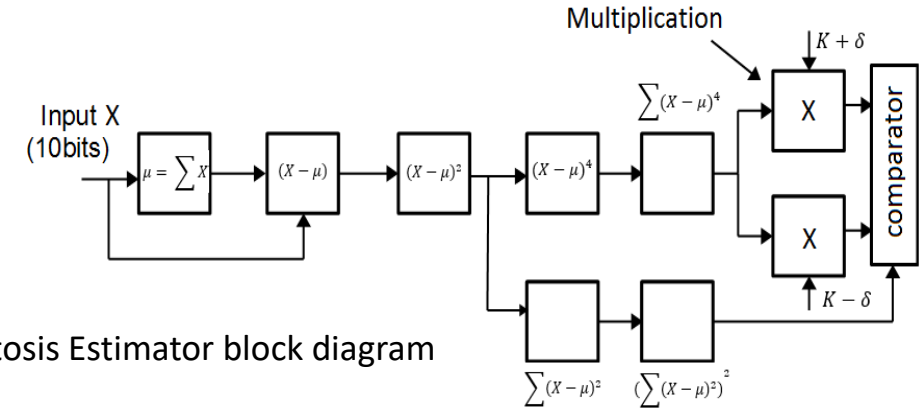
Polyphase Filter Bank's (PFB) Single core 8-tap filter with 10-bit input lines and 10-bit coefficients (2/2)



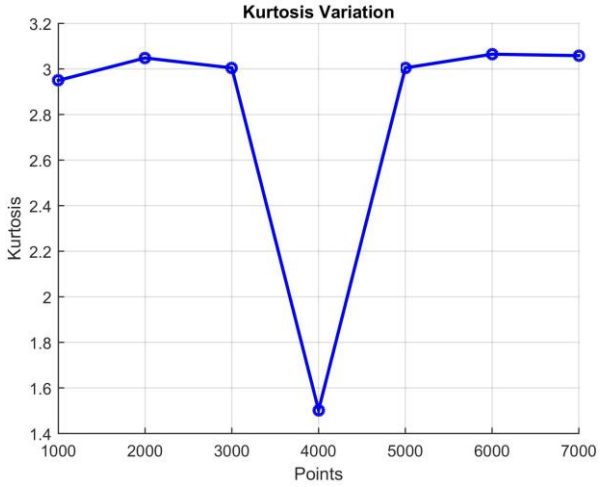


- 1024 sub-band PFB
- 8-tap filter with 10-bit coefficients
- Noise floor below 60dB
- Total DSP power ~150mW

Kurtosis Variation Over Introduction of Sinusoidal Tones



Kurtosis Estimator block diagram



Kurtosis estimator block simulation showing an RFI detection during the sampling pints 3000 to 5000. A single tone sinusoidal input signal was fed to the system during this time. No other input was provided.

Kurtosis Calculation : K = $\frac{\sum(X-\mu)^4}{(\sum(X-\mu)^2)^2}$ can be can be also evaluated as

$$(K+\delta)*(\sum(X-\mu)^2)^2 > \sum(X-\mu)^4 > (K-\delta)*(\sum(X-\mu)^2)^2$$

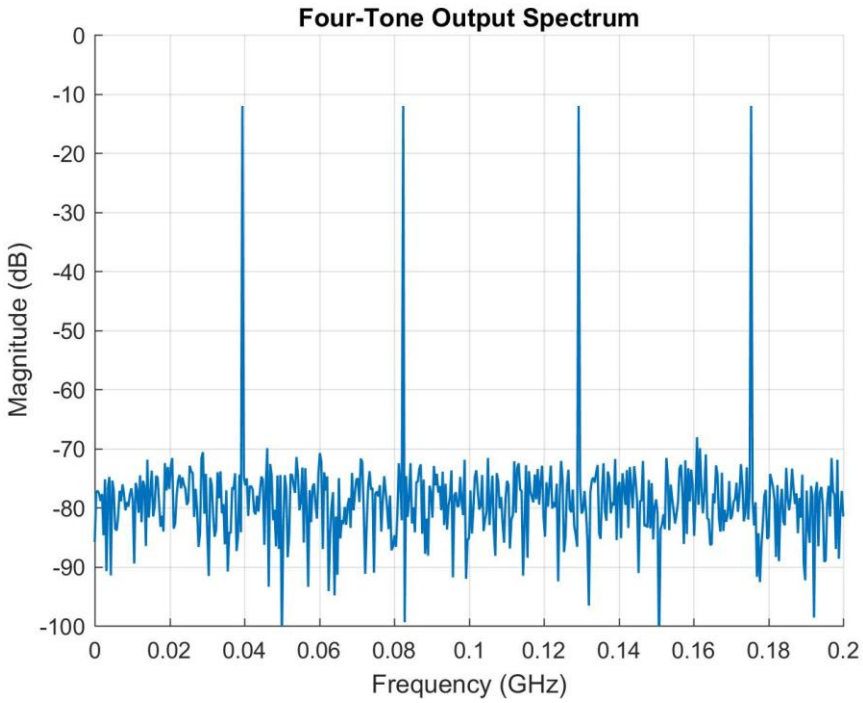
K = Kurtosis Value

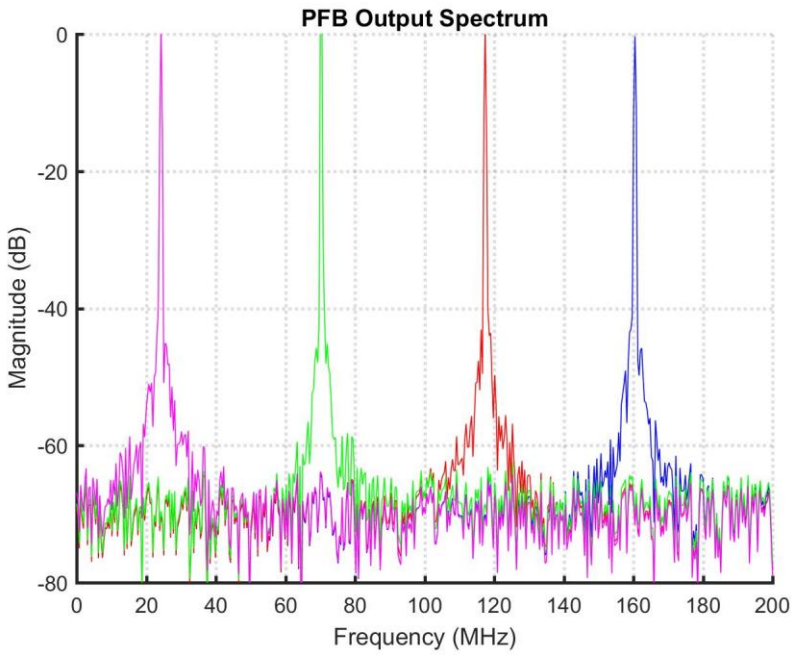
X = input data

μ = mean of N input (X) samples

δ= estimation error

ADC + PFB multitone response





- ADC Multitone response has noise floor below 70dB
- Sub-bands' FFT plots merged

Radiation Effect Mitigation

- 100 krad(Si) of total ionizing dose (TID) is the requirement of most NASA missions (Jupiter-bound missions require up to 3Mrads)
- The selected 28nm CMOS process has been tested to have inherent tolerance to 500krad(Si)
- The silicon insulator (SOI) process provides complete immunity to single-event latchup, the main concern for CMOS electronics in space
- The process also provides 10X - 20X lower single event upset (SEU) rate
- Long term on-chip bit storage devices (configuration and calibration coefficient memories) will be hardened with layout techniques (DICE latches, increased capacitance and resistance)

Summary

- We present the first low-power RFI mitigating receiver backend ASIC that pushes the state of the art significantly in terms of SWAP.
- It is designed in a 28nm process and it will be rad-hard to 500krad(Si) of total ionizing dose (TID) and immune to single event latchup (SEL).
- The ASIC includes an on-chip analog to digital converter (ADC) and a RFI detecting/mitigating digital signal processing (DSP) block.
- The ASIC is capable of processing signals with bandwidths exceeding 1.0GHz. The ADC has a 10-bit, 2 GS/s radiation-hard successive approximation register (SAR) architecture. The DSP block includes a 1024-channel polyphase filter bank (PFB), a Fast Fourier Transform (FFT) blocks and Kurtosis detection & accumulation block.
- The total ADC power is 35.7mW (with >9 bits ENOB). The DSP will have a high degree of programmability that includes the selection/bypassing of the Kurtosis estimation, selection of the number of channels, selection of the decimation factor and selection of time spans for the accumulation of statistical averages.
- The goal is to increase the sampling rate to 5GS/s and add more programmability to number of channels. We will tapeout a test chip November 2017 and use these results for the future design.

Some Other Alphacore Programs…

…that may be of interest to you

High Speed Digitizer for Remote Sensing

ALPHACORE

Analog, Mixed Signal & RF Electronics

NASA SBIR Phase I & PHASE II

NASA need: A high-resolution, low-power, rad-hard analog-to-digital converter (ADC) suitable for NASA's remote sensing applications.

- 4b, 25GS/s, 25GHz, 400mW flash ADC with 12.5Gb/s I/Os
- I/O interface is optimized for interfacing to an FPGA
- Designed in a 28nm CMOS SOI technology
- Targets a range of NASA's remote sensing instruments, scalable for use in balloons, aircraft and satellites.
- Radiation hard up to 500krad(Si) and SEL immune

Status: Completion by Oct 2017

Specification	Alphacore's ADC
Architecture	2-channel interpolated flash
Interconnect	Chip-on-Board
Sampling rate / Input frequency	25GSPS/25GHz
Power [ADC core / entire chip with I/Os]	400mW
Radiation hardness	500krad

High Sample Rate A/D Converter

ALPHACORE

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DARPA SBIR Phase I & PHASE II

DARPA need: Low-power, high-peed ADC for phased array SoCs

- Used in phased array technologies
- End goal is a 7b, 40GS/s, 20GHz, 500mW interpolated flash ADC
- Designed in a 28nm CMOS SOI technology
- Design will be radiation hard up to 500krad(Si) and SEL immune
- First test chip containing the analog front-end and calibration circuit has been taped out in September 2016
- Upgraded version of the NASA ADC

Specification	Alphacore's ADC
Architecture	2-channel interpolated flash
Interconnect	Flip-chip
Resolution	7 bits
Sampling rate / Input frequency	40 GSPS / 20 GHz
I/O type	12.5 Gbps CML, XOR/PRBS encoded
Radiation hardness	500krad

Status: Completion by May 2019

Analog to Information Processing

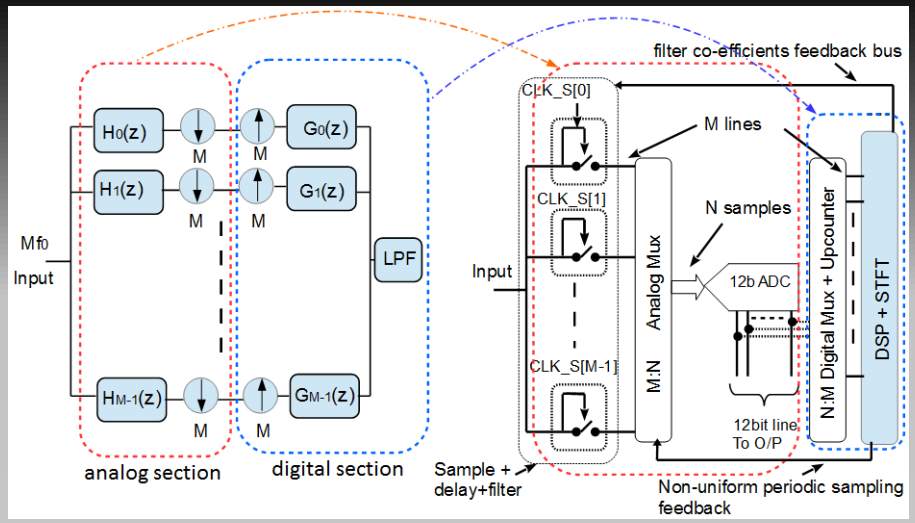
ALPHACORE

Analog, Mixed Signal & RF Electronics

Navy SBIR Phase I

Navy need: An analog to information processing approach to bypass analog-to-digital conversion that is capable of lower power consumption, smaller circuit size and does not require upfront digitization.

- Unique analog IC design that transforms RF inputs directly to useful information without off-chip digitization
- The systems forms an ADC with impressive specs:
  - ENOB > 10bits
  - Linearity > 12bits
  - Bandwidth > 10GHz
  - Core Design Power < 150mW
- Incorporates bank of filters and on-chip digital signal processing circuitry
- Applications include radar, wireless communication and optical transport networks



Status: Completed Mar 2017

And just for fun, check out…

http://nist-takingmeasure.blogs.govdelivery.com/weird-signals-listening-eclipse/

‘W’eird Signals: Listening in on the Eclipse

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BY JILL NELSON ON AUGUST 15, 2017

ADVANCED COMMUNICATIONS, ELECTRONICS, ENGINEERING, PHYSICS

Earth's ionosphere. Credit: NASA

Two years ago, I had never heard of the WWVB radio station. Today, it’s one of my favorites, but that’s not because it broadcasts a pleasant mix of Top 40 hits. (It doesn’t.)