SKARAB

AGILE 40 GBE NETWORKED FPGA COMPUTE/INSTRUMENT PLATFORM

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Designed and Manufactured by Peralex Electronics
Distributed worldwide by Cyntony

SKARAB IS READY FOR YOUR RESEARCH TODAY

- Board Support Package (BSP) on Github
  - SKA-SA software uses open source Apache Version 2 license
- CASPER Listserv development support, led by SKA-SA
- Over 100 SKARAB systems delivered to SKA-SA by Peralex
- Mature, fully qualified and shipping
  - FPGA board, power supply, cooling in 1U enclosure
  - 4 x 40 GbE QSFP+ mezzanine card
  - 4 GB Hybrid Memory Cube mezzanine card
  - New 3 GSPS 14-bit ADC mezzanine card
- Cyntony distributes worldwide

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HOW WILL YOU USE SKARAB? AS A...

CORRELATOR

SPECTROMETER

BEAMFORMER

RADAR

NEW GIZMO?

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SKARAB

Extreme FPGA computing
Real-time reconfiguration
Massively networkable
Wideband A/D conversion
Highly power efficient

Concept by SKA-SA
Design and Manufacture by
Peralex Electronics

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DESIGN AND VERIFICATION

- Peralex won RSA tender deliver 300 SKARABs for MeerKAT
- Extensive signal integrity analysis and verification
  - 10.3125 Gbps over 7m on 128 links.
- CFD and real-world thermal analyses
- MTBF analysis fed back into design to maximize reliability
  - 110,000 hours at 44 degC
- Thorough environmental design verification tests
  - EMC/RFI, temperature, shock and vibration

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MANUFACTURING AND TEST

- Peralex assembles units and performs automated final tests
  - Internal and supply chain quality management
  - Optimized assembly fixtures and test harnesses
  - Thermal stress screening to eliminate infant mortality
- Key components get supplier tests
  - PCB delamination stress testing
  - X-ray/AOI inspection of all PCB assemblies

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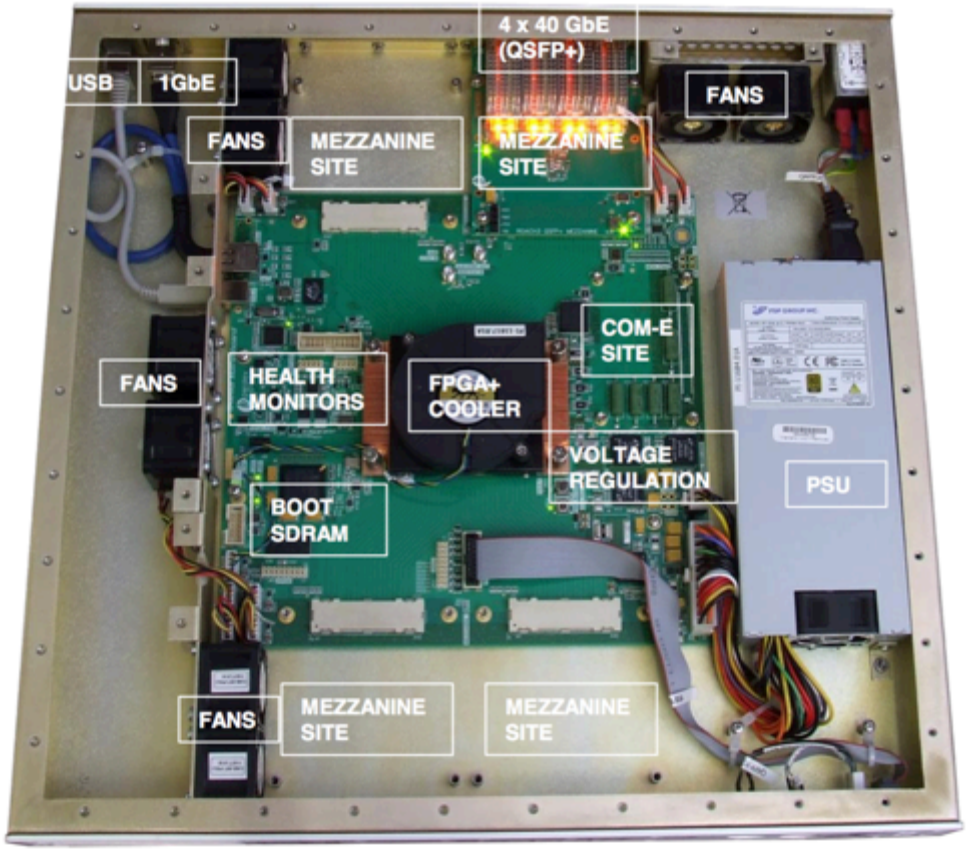
Square Kilometer Array Reconfigurable Application* Board

Under the hood

*SKARAB is NOT application specific



SKARAB SPECS

Xilinx Virtex 7 FPGA
- XC7VX690T-2-FFG1927
- 693,120 logic cells
- 3600 DSP slices
- 54 Mb RAM
- 80 x SERDES channels

Four Mezzanine sites
- 1.28 TBPS total throughput
- 4 x 40 GbE QSFP+
- Quad 3 GSPS ADCs optional
- Hybrid Memory Cube optional

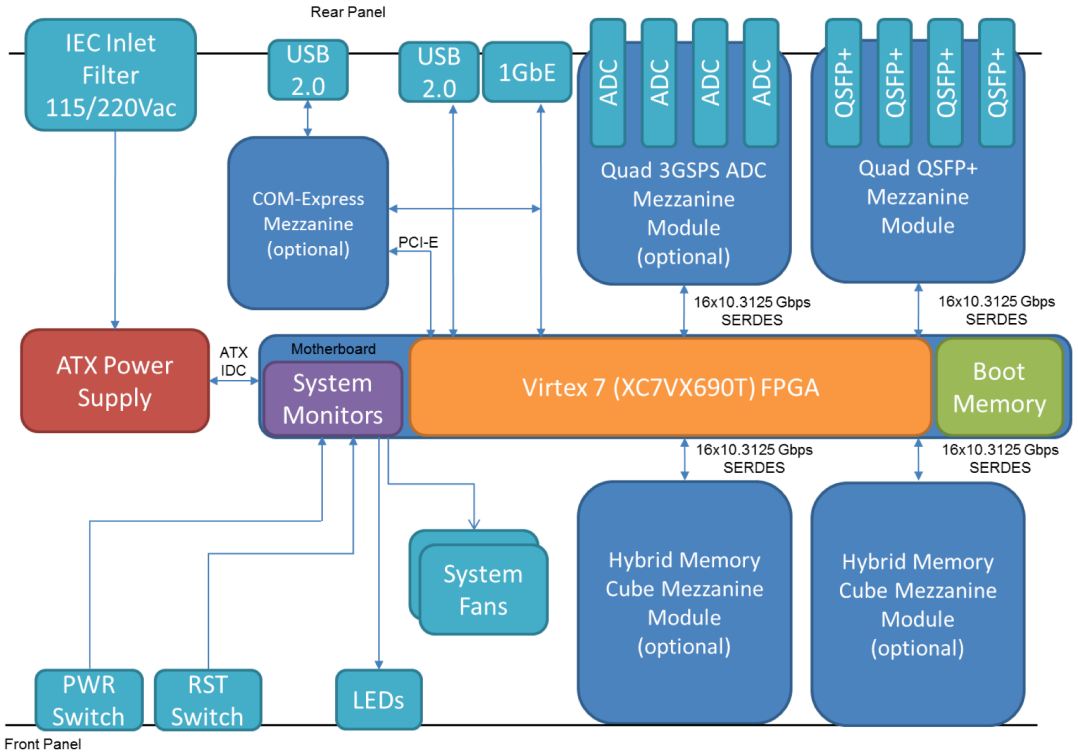
COM-Express mezzanine optional

GBE management interface
- Remote monitoring/shutdown

Energy efficient (45 W floor)

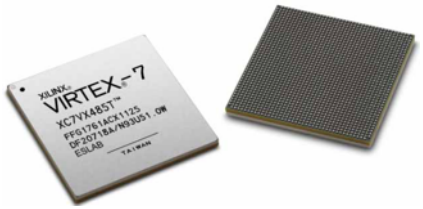
1U rackable form factor

5 to 40 deg C operating temp range



SKARAB FPGA: VIRTEX

- 693120 Logic Cells
- 80 x SERDES
  - 64 for mezzanine I/O
  - 1 for COM-Express site
- 1470 x 36Kb RAM Blocks (~52 Mb)
- 3600 DSP Slices
- 1927 pins



	Part Number		XC7VX690T
	EasyPath™ Cost Reduction Solutions[1]		XCE7VX690T
Logic Resources	Slices		108,300
	Logic Cells		693,120
	CLB Flip-Flops		866,400
Memory Resources	Maximum Distributed RAM (Kb)		10,888
	Block RAM/FIFO w/ ECC (36 Kb each)		1,470
	Total Block RAM (Kb)		52,920
Clocking	CMTs (1 MMCM + 1 PLL)		20
I/O Resources	Maximum Single-Ended I/O		1,000
	Maximum Differential I/O Pairs		480
Integrated IP Resources	DSP Slices		3,600
	PCIe® Gen2[2]		—
	PCIe Gen3		3
	Analog Mixed Signal (AMS) / XADC		1
	Configuration AES / HMAC Blocks		1
	GTX Transceivers (12.5 Gb/s Max Rate)[3]		—
	GTH Transceivers (13.1 Gb/s Max Rate)[4]		80
	GTZ Transceivers (28.05 Gb/s Max Rate)		—
Speed Grades	Commercial		-1, -2
	Extended[5]		-2L, -3
	Industrial		-1, -2
	Package[6]	Dimensions (mm)	GTH)
Footprint Compatible	FFG1157 / FFV1157[7]	35 x 35	0, 600 (0, 20)
	FFG1761 / FFV1761[7]	42.5 x 42.5	0, 850 (0, 36)
	FHG1761	45 x 45	
	FLG1925	45 x 45	
	FFG1158 / FFV1158[7]	35 x 35	0, 350 (0, 48)
Footprint Compatible	FFG1926	45 x 45	0, 720 (0, 64)
	FLG1926	45 x 45	
	FFG1927 / FFV1927[7]	45 x 45	0, 600 (0, 80)
Footprint Compatible	FFG1928	45 x 45	
	FLG1928	45 x 45	
Footprint Compatible	FFG1930	45 x 45	0, 1000 (0, 24)
	FLG1930	45 x 45	

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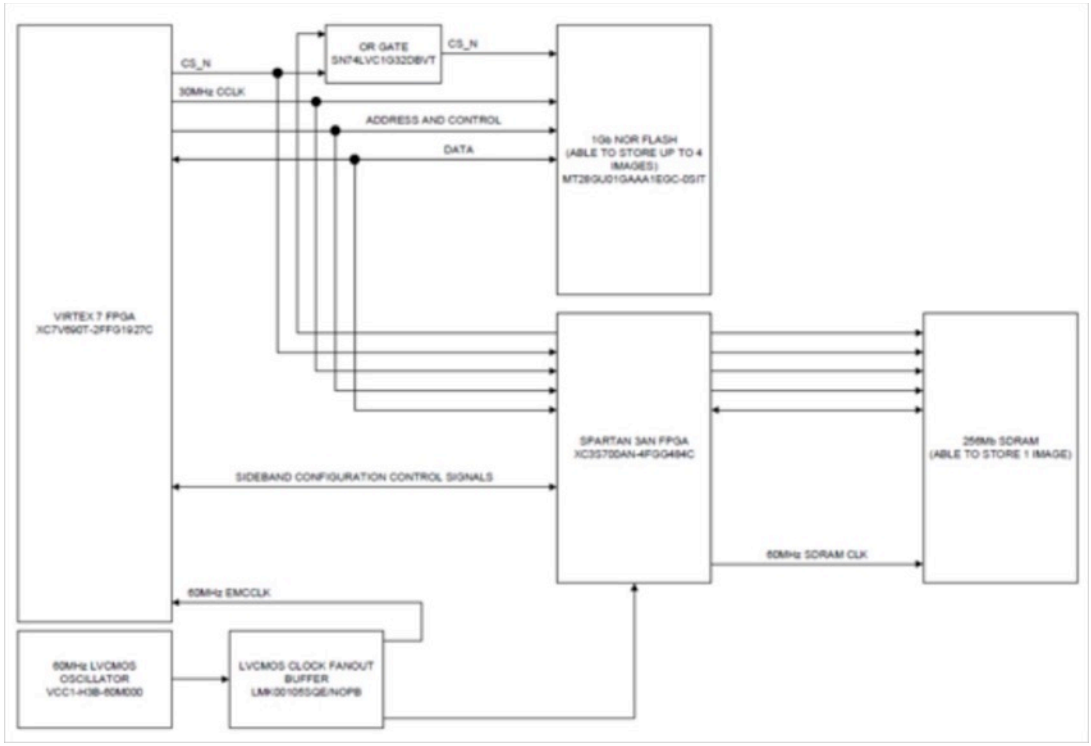
FPGA (RE)CONFIGURATION

- On power-up, FPGA boots from NV flash
- Can then be rebooted over 1 GbE using SDRAM-based high-speed boot mode
- Boots in < 1 second for rapid reconfiguration



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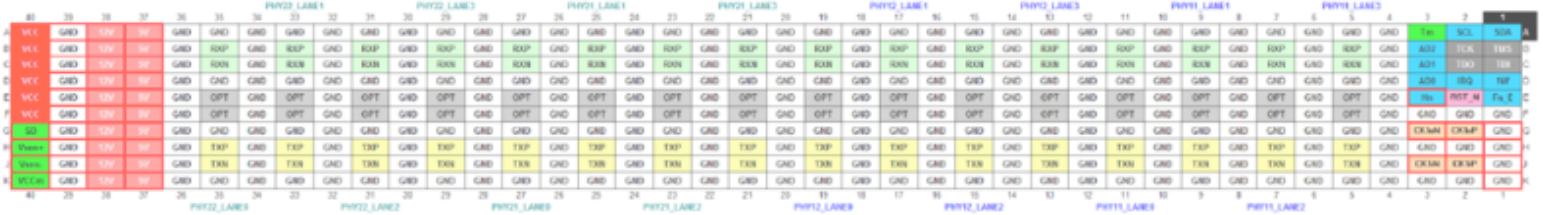
FOUR MEZZANINE SITES

- 400 pin MEG-array connector
  - Capable of 28 Gbps
- 16 x ~10 Gbps SERDES
- 1-Wire Interface (config PROM)
- I2C management interface
- JTAG test interface
- High speed clocks
- Power (12V, 5V, 3.3V)



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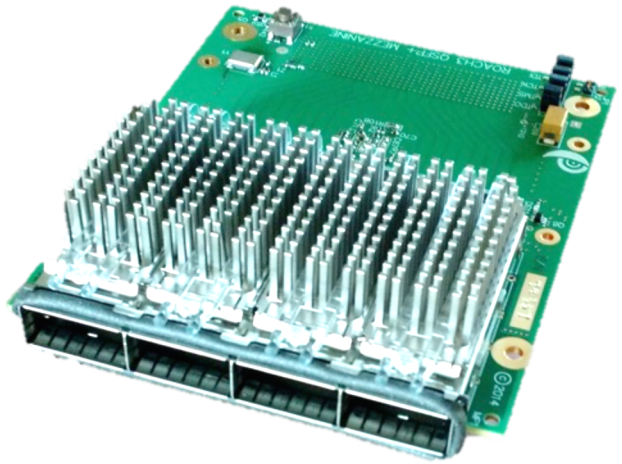
4 x 40 GbE QSFP+ MEZZANINE CARD

- 4 x QSFP+ interfaces
  - 16 x 10 Gbps SERDES
  - Copper, AOC, SR & LR fiber
- 32-bit ARM μC (mgnt & boot)
- Configuration PROM
- Clock generation
- Thermal sensor
- Design/Manufacture by Peralex



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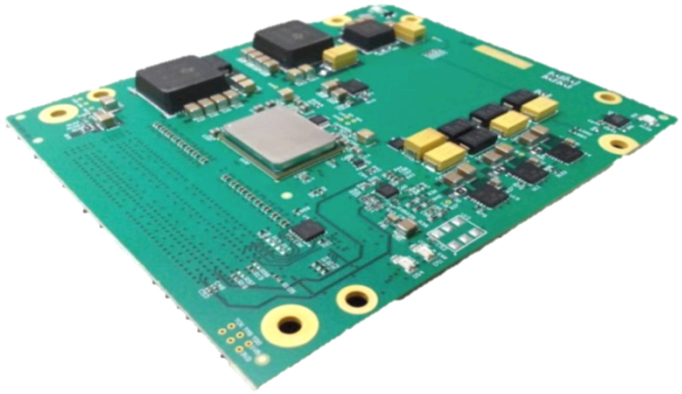
HYBRID MEMORY CUBE MEZZANINE CARD

- 4 GB Micron HMC chip
- 10 Gbps x 16 SERDES to FPGA
- Relative to DDR3/4:
  - Higher bandwidth
  - More energy efficient
  - More parallel
- Relative to QDR SRAM & Bandwidth Engine
  - Larger capacity
- Designed by SKA-SA
  - Manufactured by Peralex



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ADC32RF45X2 MEZZANINE

- 2/4 3 GSPS 14-bit ADC Channels
  - 600 MHz BW
  - 22 W power consumption at 3 GSPS
  - optional PGA
- On-board digital down converters
  - Two per ADC & dual band mode
  - Three independent NCOs/DDC*
- High perf. 3 GHz sample clock generator
  - Phase synchronous DAQ across channels/boards
- Dedicated sub-system management μP
- JESD204B interface to FPGA
- Design/Manufacture by Peralex

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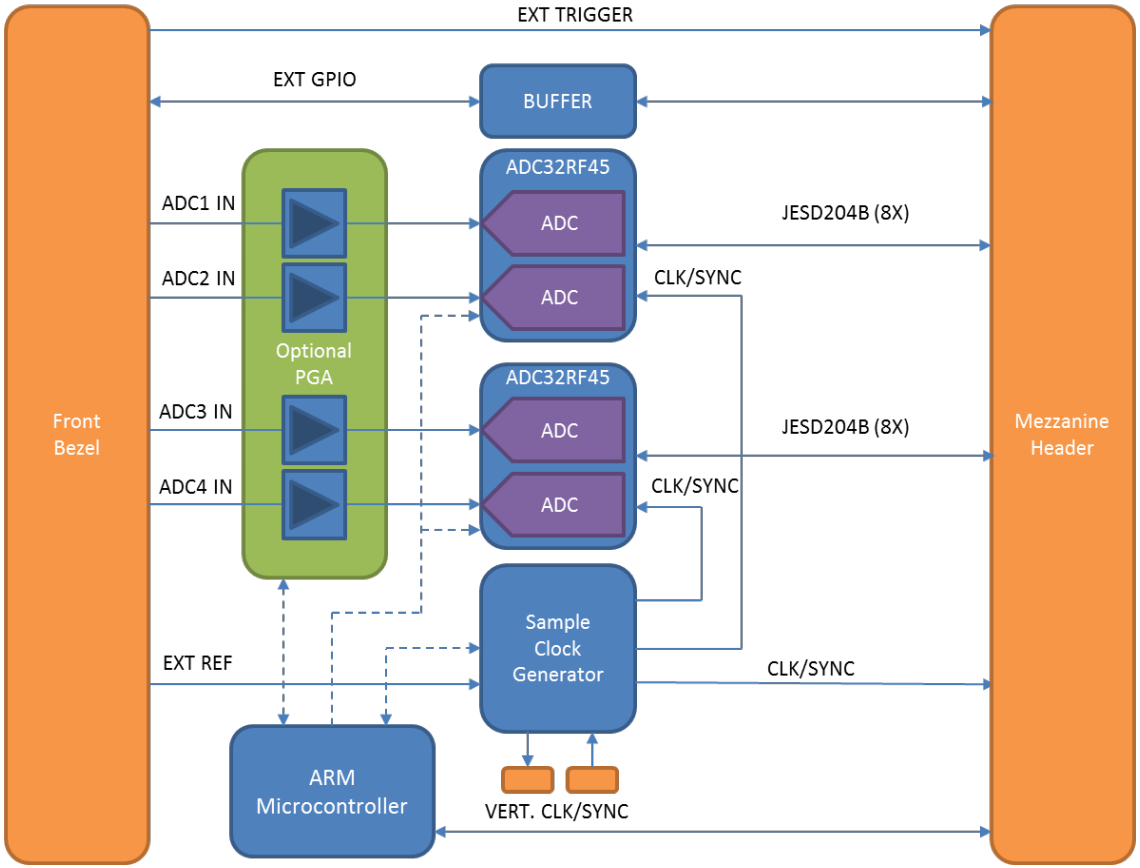
ADC32RF45X2 BLOCK DIAGRAM



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ADC MEZZANINE CONFIGURATION OPTIONS:

- Two ADC chip variants, one or two chips per mezzanine
  - TI ADC32RF45 – Full 1.5 GHz Nyquist bandwidth using DDC bypass
  - TI ADC32RF80 – DDC not by-passable, max BW of 600 MHz
    - lower priced
- Programmable Gain Amplifier (PGA) vs balun-coupled input
  - PGA gain range: ~ -6 to +15 dBm
  - PGA lowers required full scale drive strength (at the expense of NF)
  - Balun coupling recommended when operating at higher analog input frequencies (e.g. 2.0 GHz)

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TI ADC23RF45 CHIP SPECS

- Dual-Channel, 14-Bit, 3.0-GSPS ADC
  - Input Full-Scale: 1.35 VPP
  - RF Input Supports Up to 4.0 GHz
  - On-chip 50 Ohm Input Termination
- On-chip Digital Down-Converters:
  - Up to 4 DDCs (Dual-Band Mode)
  - Up to 3 Independent NCOs per DDC
- On-chip Dither
- Aperture Jitter: 90 fsec
- Noise Floor: –155 dBFS/Hz
- Channel Isolation: 95 dB at Fin = 1.8 GHz
- Programmable On-Chip Power Detectors
  - Alarm Pins for AGC Support
- On-chip Over-voltage Protection Clamp
- JESD204B Interface
  - 4 Lanes Per Channel at 12.5 Gbps
- Support for Multi-Chip Synchronization
- Spectral Performance (Fin = 900 MHz, –2 dBFS)
  - SNR: 60.9 dBFS
  - SFDR: 67 dBc HD2, HD3
  - SFDR: 77 dBc Worst Spur
- Spectral Performance (Fin = 1.78 GHz, –2 dBFS)
  - SNR: 58.8 dBFS
  - SFDR: 66 dBc HD2, HD3
  - SFDR: 75 dBc Worst Spur

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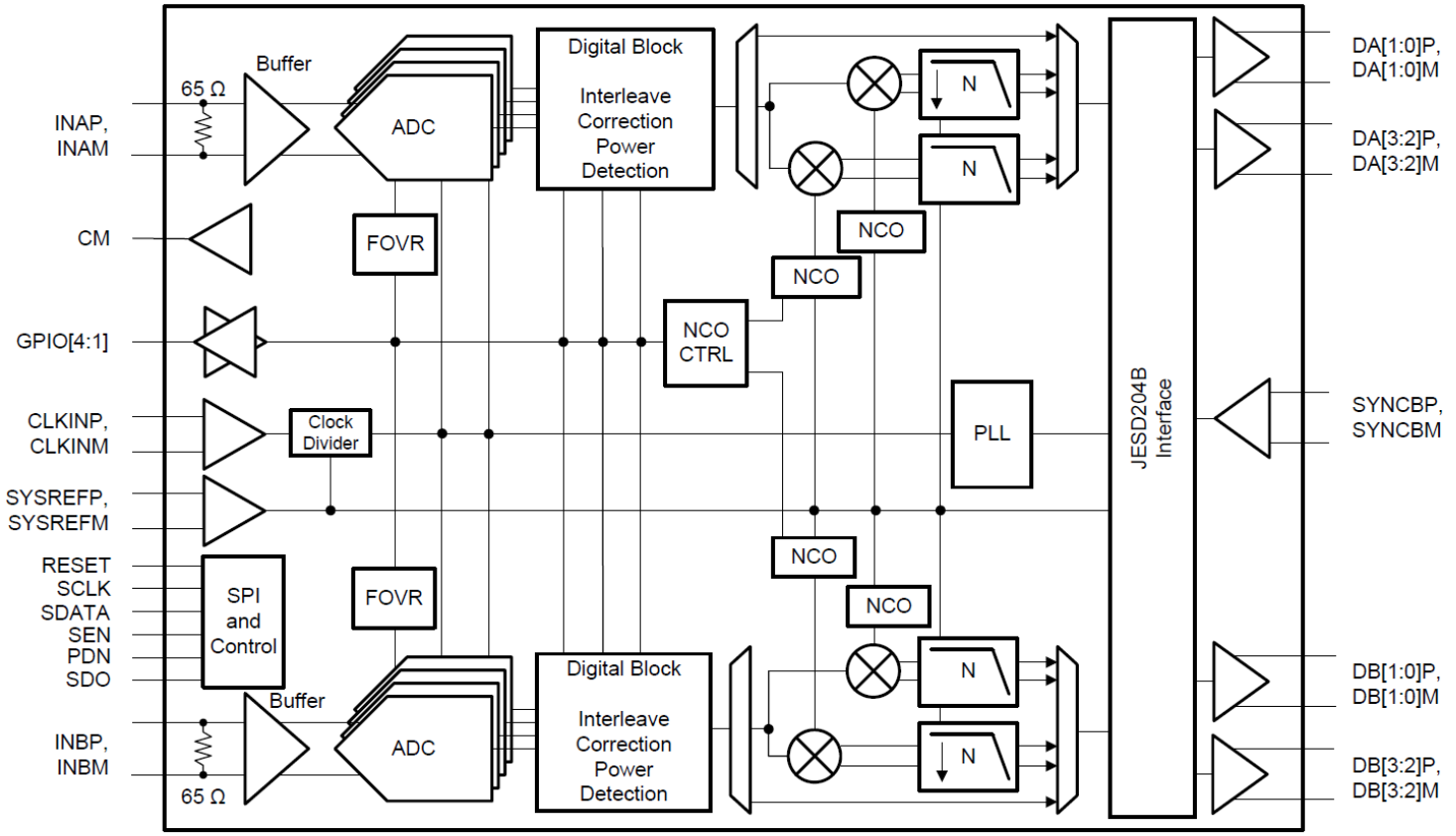
TI ADC32RF45 DUAL ADC BLOCK DIAGRAM



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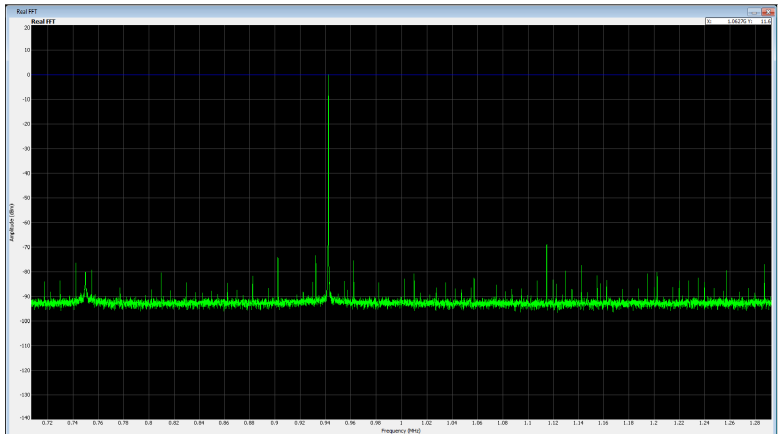
SKARAB ADC32RF45X2

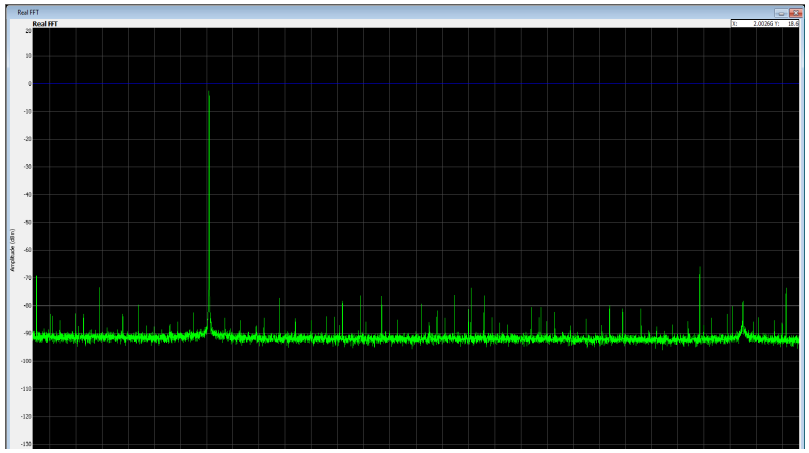


Test Case 1:
Input Frequency: 942.5 MHz
Input amplitude: -10 dBFS
Sample rate: 3.0 GSPS
Full Scale: 9.375 dBm
DDC: Decimate-by-4
FFT: 16384
Average: 5
PGA: none

Result <<
Single-tone spurious: -71.725 dBc
IMD3: 76.435 dBc @ -8dBFS
FFT Noise Level: -94.125 dBm

Test Case 2:
Input Frequency: 1842 MHz
Input amplitude: -1 dBFS
Sample rate: 3.0 GSPS
Full Scale: 12.525 dBm
DDC: Decimate-by-4
FFT: 16384
Average: 5
PGA: none

Result >>
Single-tone spurious: -63.125 dBc
IMD3: 68.375 dBc @ -8dBFS
FFT Noise Level: -81.025 dBm



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UNIT MANAGEMENT

- Autonomous/programmable fan control
  - Auto shutdown on fault
- Autonomous voltage/current/fan monitoring and protection
- Fault recording
  - Always-on USB access to fault log
- USB/JTAG access to compliant devices throughout
- Serial port interface to Microblaze processor

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PLATFORM MANAGEMENT

- Services on all Ethernet interfaces
  - DHCP
  - Ping
  - Health monitoring
- Network-based FPGA Configuration
  - High-speed via 1 GbE or 40 GbE interface (< 1 second)
- Board Support Package provides the code

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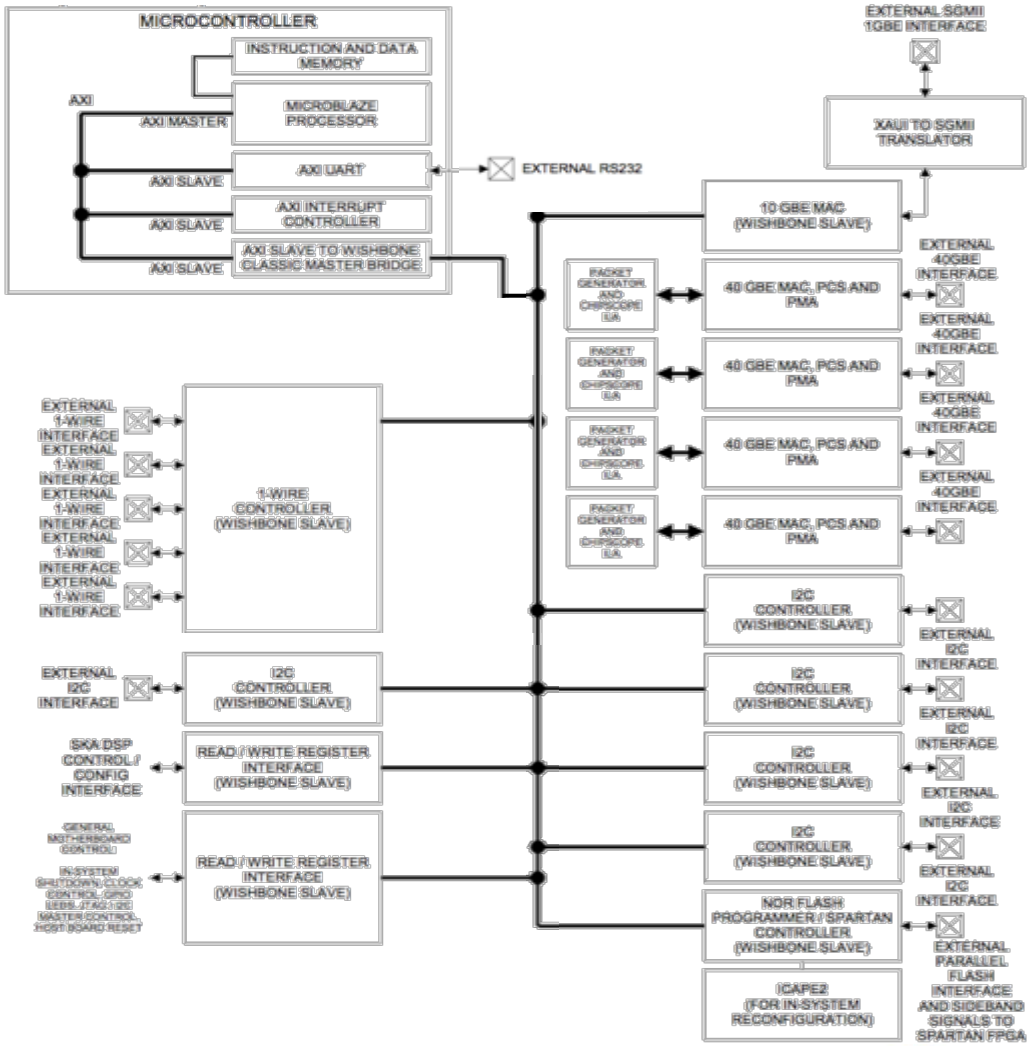
SOFTWARE SUPPORT

- Includes open-source Board Support Package (BSP)
  - HDL code for Xilinx Vivado suite (customer supplied)
  - FPGA Firmware for 1 GbE MAC, 40 GbE MAC & PHY, HMC, ADC
  - Microblaze soft-processor, Wishbone peripheral bus and 1-Wire
  - Fan control, air speed/thermal/voltage/current monitoring
- Includes Network Management
  - Windows/Linux C++ reference code and executables to manage unit(s) via a network-attached PC
- Support for open-source Yellow Blocks and JASPER code via CASPER listserv

BSP BLOCK DIAGRAM

- Microblaze soft μC
- Wishbone bus/SDRAM
- 10/40 GbE PHY, MAC
- I2C, Register R/W
- FLASH controller
- ICAPE2 configuration



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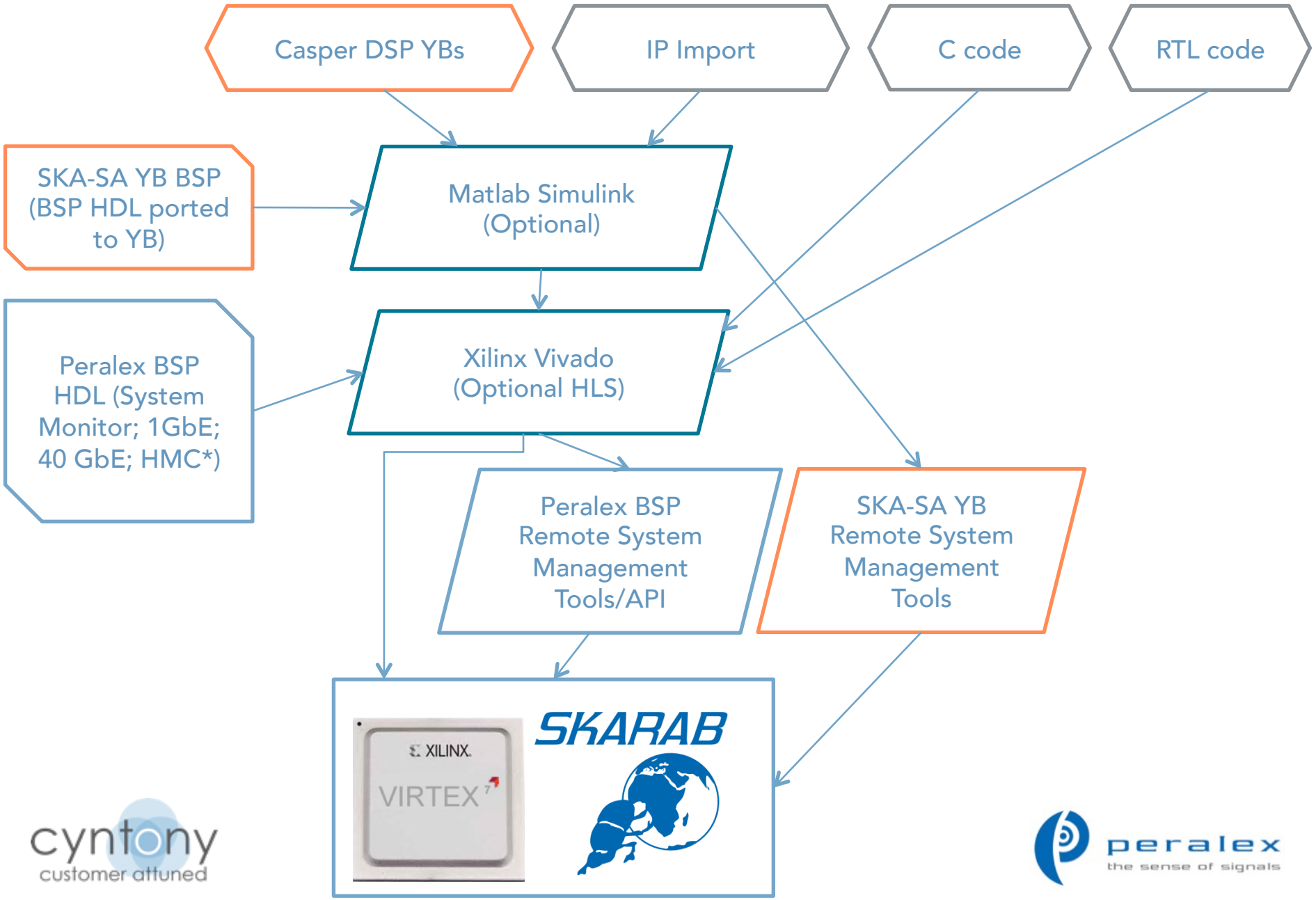
TOOLFLOW DIAGRAM



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ABOUT PERALEX

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- Founded 1987, located near Capetown, South Africa
- Pioneer in high-end DSP and SDR
- Designer and manufacturer for sophisticated customers:
  - South African National Space Agency, SKA-SA (MeerKAT), CapeRay
  - GEW Technologies, L-3 Communications, Cassidian
- High Performance Products
  - Wideband radio receivers, FPGA extreme computing
  - ADC PCBAs, DSP PCBAs
  - Associated firmware and software
- Applications Expertise
  - Spectrum Monitoring, Direction Finding, Signal Analysis

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- Mature, fully qualified, in production and shipping
- Over 100 SKARAB systems delivered to SKA-SA for MeerKAT
- CASPER Listserv development support, actively led by SKA-SA
- Board Support Package (BSP) on Github
- Come see the ADC Mezzanine in action in the demo room

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CONTACT INFORMATION

Cyntony is the premier worldwide distributor for Peralex

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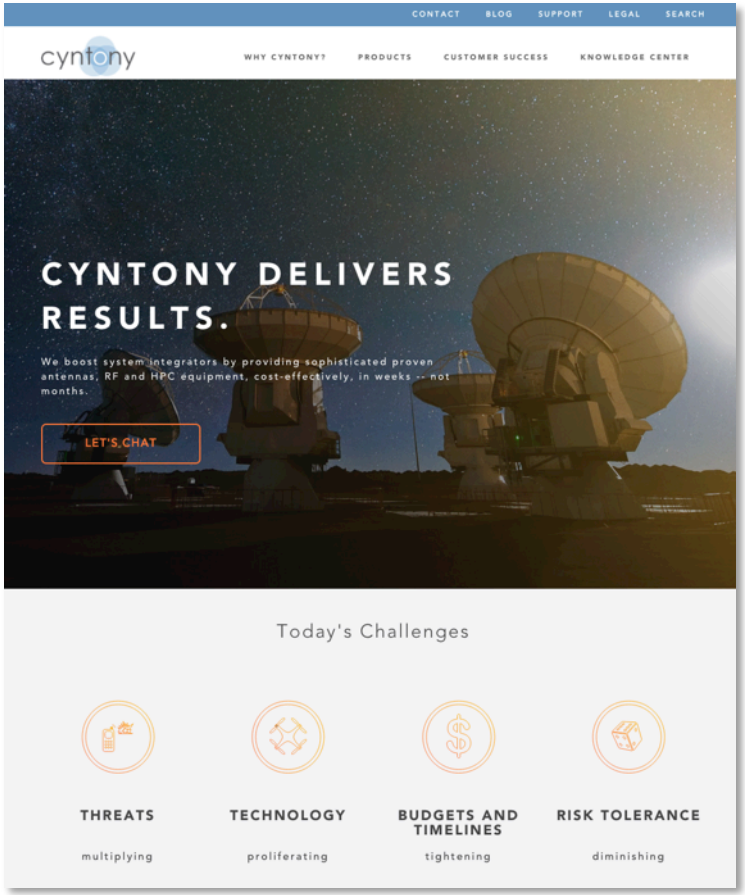

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