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ADC Crosstalk Measurements with SNAP for OVRO-LWA

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Introduction

The LWA (Long-Wavelength Array), located at Owens Valley Radio Observatory, is a powerful and sensitive radio telescope. OVRO-LWA needs very good signal transmission with minimal spurious emissions carried through its signal chain.

The telescope receives analog radio signals from space, then interprets them as digital data that can be computationally analyzed to gain a better understanding of what that data means. A high-level description of the flow of information in the LWA is as follows:

Analog receiver → analog-to-digital conversion (ADC) → short-timescale FPGA processing → long-timescale GPU processing

In order to minimize unwanted effects, some parts of the signal chain are being redesigned. This includes possible changes in the ADCs employed, the FPGA used, or the circuitry linking the two. A variety of options are available for the new hardware, including several boards from the CASPER[1] collaboration. Currently, the LWA uses CASPER ADC16x250-8 RJ45 rev 1 boards with HMCAD1511 ADC chips. A different CASPER board, or a new combination of ADC and FPGA hardware from multiple platforms, may be used. Among the candidate replacement boards is SNAP[2] (Smart Network ADC Processor). In order to determine the viability of retooling the SNAP board for this purpose, the performance characteristics of its ADC hardware have been tested.

Test Setup

The key ingredient for these tests is the SNAP board, which will allow for testing of its HMCAD1511[3] ADC chip. The SNAP board accepts 12 analog input signals (3 discrete ADC chips with 4 inputs each). Here we measure the cross-talk among input signals by sending a single test signal (a sine wave) for digitization to one input of the board, along with a small dithering signal applied to the remaining inputs. A photograph and block diagram of the test configuration is included below:

[1] https://casper.berkeley.edu

[2] https://casper.berkeley.edu/wiki/SNAP

[3] http://www.analog.com/media/en/technical-documentation/data-sheets/hmcad1511.pdf

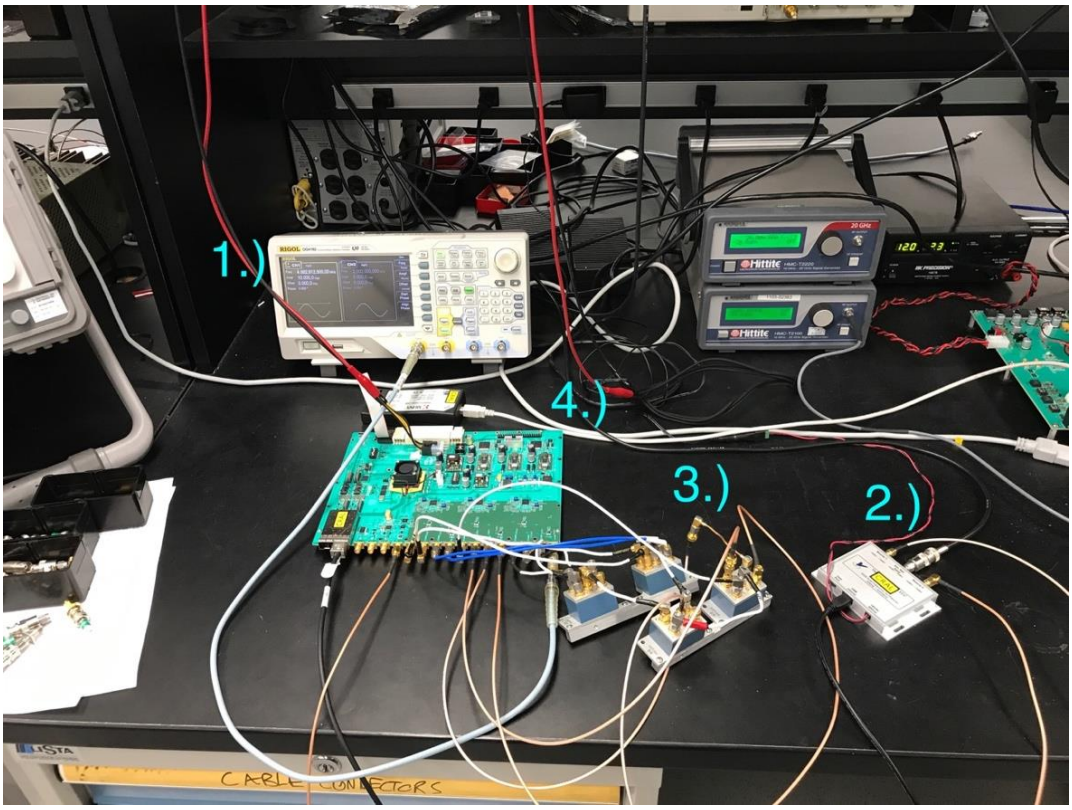
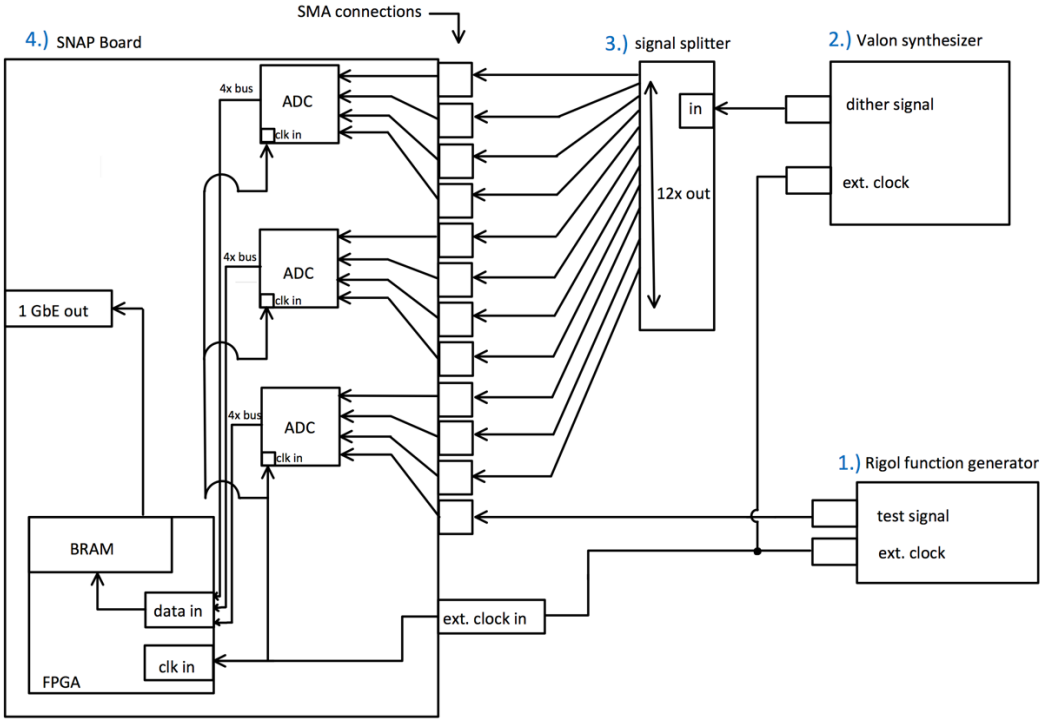


Figure above shows the configuration for SNAP testing. A block diagram of the setup is shown below.



This block diagram corresponds to the photograph above; numbered hardware matches the numbers in the photograph. Note that the Valon 5009 AK04QYPN synthesizer, the Rigol DG4162 function generator, the HMCAD1511 ADC chips, and the Xilinx XC7K160T-2FFG676C FPGA are locked to the same clock source.

In the test setup shown above, each SMA input to the SNAP board is driven with a signal: one input is driven with a sine wave test signal which is meant to bring one 8-bit ADC nearly all the way through its full range of 256 digital values (-128 to +127), test signal voltage is therefore set so that nearly the maximum rated value of 2V peak-to-peak is seen at the ADC input circuit. The remaining inputs are driven with 11 identical copies of a small dithering signal. These dithering signals allow for detection of a very weak cross-coupled signal, even if its amplitude is smaller than one quantization bin.

The most useful way of understanding the outputs produced by the SNAP ADCs is by examining frequency spectra. In the field, frequency spectrum plots allow for separation and measurement of each spectral component of a particular physical phenomenon occurring in space. In the lab, these spectra allow us to carefully search for and mitigate unwanted electrical or digital-signal processing-related effects.

A common yet effective way of examining a waveform's frequency content is to take the Fourier transform of a waveform by applying the Fast Fourier Transform (FFT) algorithm to a set of digital data representing that waveform. The Xilinx Kintex-7 FPGA on the SNAP board is capable of capturing a 16384-byte snapshot of digital data representing an input signal for each of the SNAP's 12 ADCs simultaneously. This means that we can obtain an 8192-channel FFT of each of the 12 input signals. These spectra are produced outside the SNAP board by taking an FFT of the raw ADC data after it's imported to MATLAB or Python.

The frequencies of the test signal and the dithering signals were carefully selected in order to ensure that all ADC responses to the dithering signal (including harmonics present in that signal as well as spurs produced by non-ideal behavior of the ADC) are at frequencies that are significantly different from each test frequency. Each of these signals are in the middle of one of the 8192 FFT channels, so they ideally should produce a response in only that FFT channel. These test frequencies and the way they were determined are summarized in the table below:

Quantity	*Symbolic Representation*	*Numerical Representation*
Clock Frequency (MHz):	f_c	200
FFT Resolution (MHz):	$df = f_c / 16384$	0.0122070312500
Dither Frequency (MHz):	$f_d = 3000*df$	36.62109375000
Test Frequency 1 (MHz):	$(200 * f_c) / 8192$	4.8828125
Test Frequency 2 (MHz):	$(500 * f_c) / 8192$	12.207031250
Test Frequency 3 (MHz):	$(2000 * f_c) / 8192$	48.828125000
Test Frequency 4 (MHz):	$(4000 * f_c) / 8192$	97.65625000

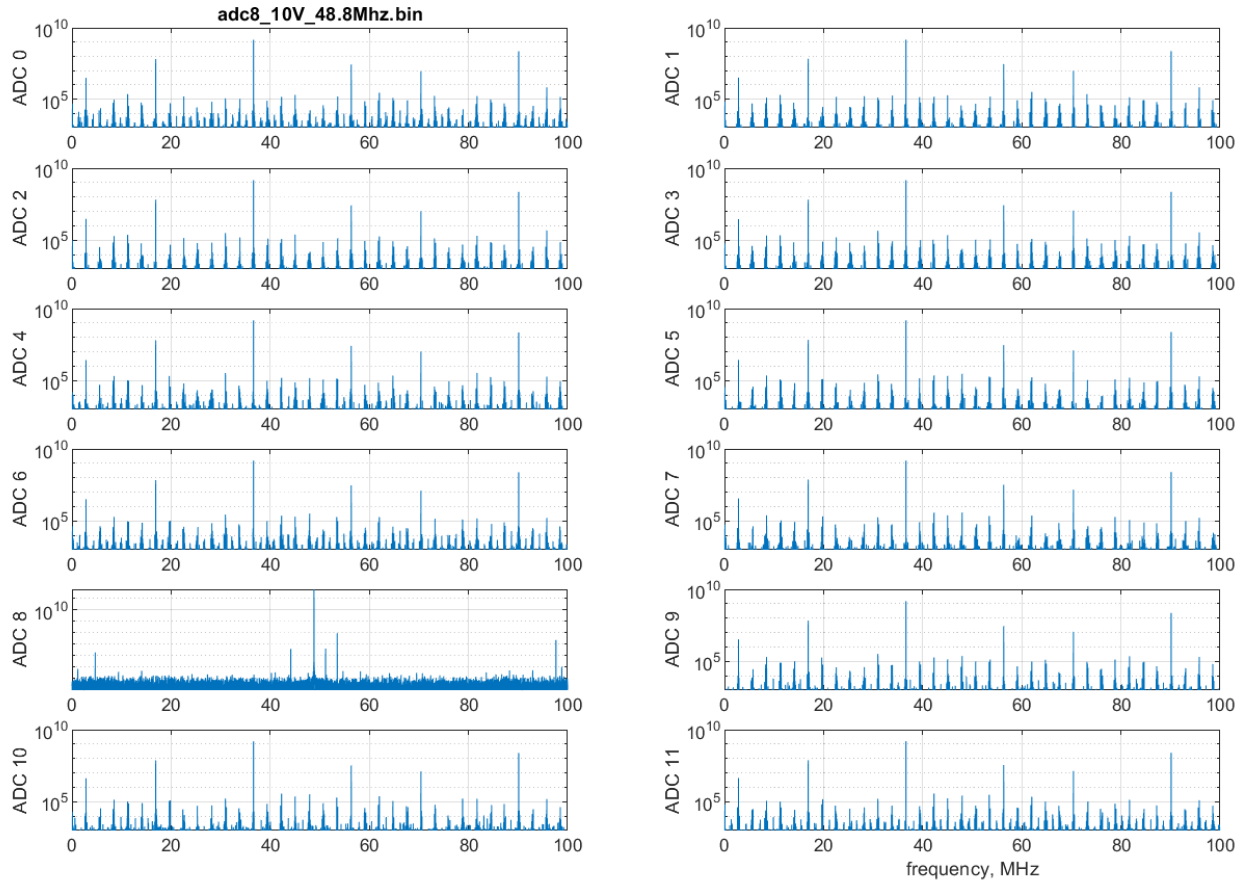
The ADC samples a time-continuous analog signal and quantizes it into a finite number of digital bins, thereby necessarily introducing a small amount of quantization error, which is essentially a rounding error between the sampled analog signal value and the quantized digital representation. The signal-to-noise ratio (SNR) for an ideal ADC is given by[4] $SNR = (6.02\text{dB})Q + 1.76\text{dB}$, where Q is the number of bits in the ADC and 2^Q is the number of digital levels it can represent. This result assumes a signal strong enough that the quantization error is uniformly distributed over [-0.5, +0.5] quantization bin. . For the 8-bit HMCAD1511, the ideal SNR is therefore 49.92dB. A comparison of this value with the typical value of 49.9dB stated in the HMCAD1511 datasheet at 250MHz in 4-channel mode shows that the ADC is nearly perfect.

[4] Ching Man, "Quantization Noise: An Expanded Derivation of the Equation, SNR = 6.02N +1.76dB." Analog Devices Mini Tutorial MT-229, 2012. www.analog.com/media/en/training-seminars/tutorials/MT-229.pdf

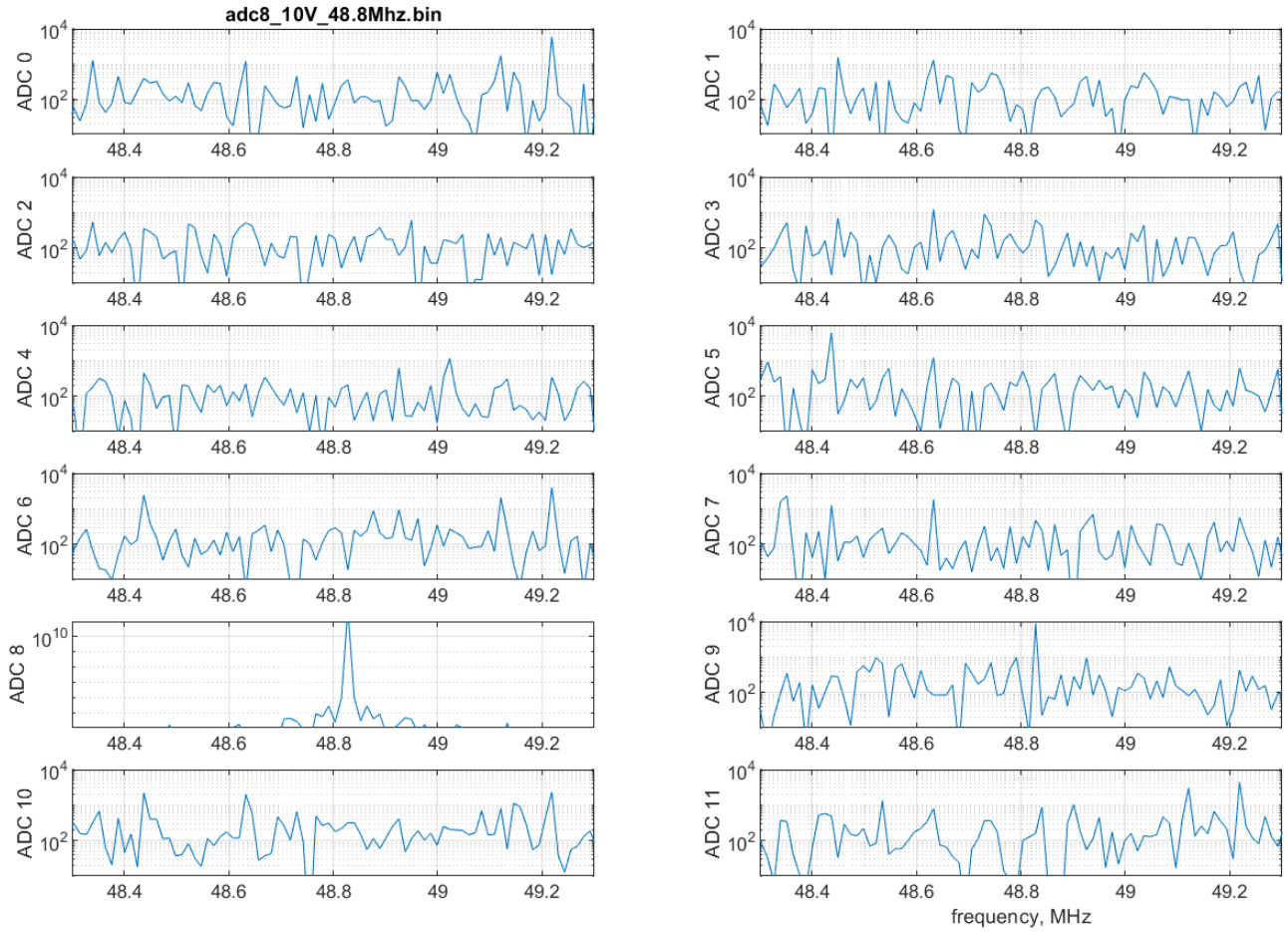
The noise power represented by the SNR figure is evenly distributed across the entire Nyquist bandwidth. Consequently, with the 8192-channel spectra measured here, the noise power in a single channel is less than the total noise power by a factor of 8192 (39.1339dB); it should therefore be possible to detect signals down to a theoretical SNR limit of 88.98dBc. The HMCAD1511 data sheet claims typical cross-talk of ~70dBc in quad-channel mode.

Results/Discussion

Some example frequency spectra gathered from the SNAP board are shown below:



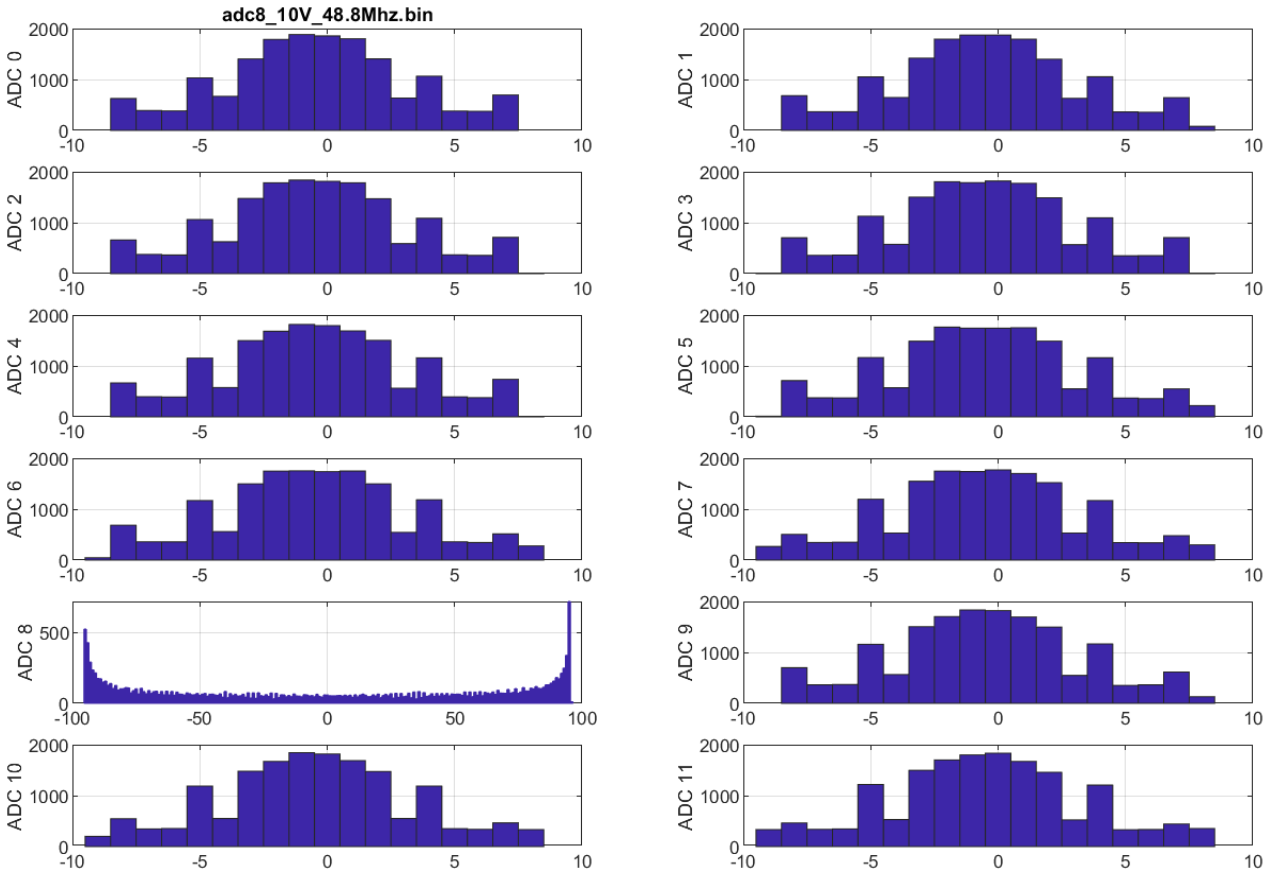
Frequency spectra from a sample of data captured by each SNAP ADC. ADC 8 is driven with a ~2V test signal at ~48.8MHz, bringing the digital output range near the signed 8-bit maximum of +/- 127. Each other ADC shows the output for a small dithering signal of frequency ~36.6 MHz.



Zoomed view of the same frequency spectrum pictured above. Note the ~48.8MHZ signal in ADC8, and the corresponding cross-talk spur in the adjacent ADC channel 9. Non-adjacent channels appear to experience minimal effects from cross-talk.

This test frequency of ~48.8MHz, as well as the other test frequencies used, were selected such that they align in the center of one of the 8192 FFT channels in order to minimize the effects of DFT leakage (wherein the sidelobes of the frequency response function spuriously add power to another channel due to imperfect alignment) and scalloping loss (attenuation of measured value for a frequency component falling partway between FFT bins). The frequency spectra pictured above show promising performance from the SNAP board, with measurable cross-talk on the order of -70dB occurring only in adjacent ADC channels, and most other channels experiencing maximum signal levels of ~ -85dB or better (e.g. in the example above, the test tone into ADC8 is at the rightmost SMA connector, leaving ADC9 to the left as the only adjacent channel, and also the only channel where cross-talk is observable).

ADC behavior can also be elucidated by displaying the output data in histogram format, which gives a representation of the number of times each analog sample is quantized to a certain digital bin. A sample histogram produced by the SNAP board is shown below:



Sample histogram for SNAP ADCs. The horizontal axis represents the digital levels the ADC can represent, and the vertical axis is the number of quantizations at that level. ADC 8 is driven with a ~2V test signal at ~48.8MHz, bringing the digital output range near the signed 8-bit maximum of +/- 127. Each other ADC shows the output for a small dithering signal of frequency ~36.6 MHz.

This test setup produces histograms of the expected shape for the sinusoidal input signal. The dithering signal from the Valon synthesizer has substantial harmonic content, giving rise to its different histogram and many lines in its spectrum. This is acceptable since we don't necessarily need to see a shape-accurate waveform for the dithering signals, as they are meant simply to facilitate determining the presence or absence of significant cross-coupling between channels.

Similar sets of data and plots were created for all 12 ADCs at each of 4 test frequencies in order to determine how cross-coupling behavior changes with frequency. The results of these tests are summarized in the below figures showing crosstalk in dB for each channel. Note that the test signal at 97.6 MHz was limited to 5V by the capabilities of the function generator.

Crosstalk/Coupling (dB)														
Signal, raw	ADC0	ADC1	ADC2	ADC3	ADC4	ADC5	ADC6	ADC7	ADC8	ADC9	ADC10	ADC11		3x avg noise (dB)
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓		↓
97.6 MHz/5.000V test signal, +/-47 digital level														
1.4729E+11	0.00	-73.14	-89.57	-84.41	-91.66	-86.77	-90.11	-88.21	-87.62	-93.57	-81.95	-96.59	ADC0	-79.92
1.5021E+11	-71.26	0.00	-80.49	-84.21	-96.07	-86.82	-86.02	-85.55	-80.20	-85.12	-80.91	-92.49	ADC1	-80.01
1.5079E+11	-89.20	-86.63	0.00	-74.17	-92.14	-84.98	-91.34	-91.89	-88.51	-92.11	-85.76	-84.34	ADC2	-80.02
1.5174E+11	-91.68	-85.77	-72.47	0.00	-89.51	-86.81	-98.03	-94.80	-89.65	-87.84	-104.84	-89.27	ADC3	-80.05
1.4985E+11	-89.89	-84.26	-86.68	-88.15	0.00	-72.62	-86.29	-95.13	-84.52	-98.58	-86.03	-79.17	ADC4	-80.00
1.5131E+11	-88.89	-83.71	-94.35	-92.55	-71.59	0.00	-84.18	-95.97	-89.79	-93.12	-86.32	-100.33	ADC5	-80.04
1.5181E+11	-95.29	-83.50	-84.47	-89.75	-85.25	-79.09	0.00	-72.47	-88.69	-86.57	-81.10	-85.24	ADC6	-80.05
1.5256E+11	-84.65	-94.75	-87.24	-85.78	-87.02	-82.27	-73.73	0.00	-84.60	-91.23	-80.47	-86.56	ADC7	-80.07
1.4899E+11	-91.31	-84.11	-84.32	-98.57	-92.91	-94.32	-98.76	-88.61	0.00	-75.20	-96.11	-92.69	ADC8	-79.97
1.5185E+11	-101.51	-88.21	-91.84	-91.24	-85.67	-86.73	-93.39	-90.88	-72.13	0.00	-80.58	-86.11	ADC9	-80.05
1.5163E+11	-95.55	-89.56	-88.53	-90.79	-82.95	-93.17	-84.15	-86.93	-91.75	-88.55	0.00	-73.35	ADC10	-80.05
1.5153E+11	-90.21	-98.32	-85.30	-87.92	-84.56	-85.97	-80.79	-88.51	-85.42	-90.04	-74.85	0.00	ADC11	-80.04
48.4 MHz/10.000V test signal, +/-95 digital level														
6.1293E+11	0.00	-79.31	-101.88	-92.81	-89.22	-95.70	-96.75	-95.31	-87.60	-88.78	-87.90	-92.93	ADC0	-86.11
6.1515E+11	-78.45	0.00	-90.25	-86.59	-89.80	-88.68	-94.43	-92.77	-94.80	-91.29	-95.00	-94.91	ADC1	-86.13
6.1705E+11	-93.01	-90.58	0.00	-81.41	-97.78	-93.52	-92.43	-89.78	-103.39	-93.66	-84.94	-109.92	ADC2	-86.14
6.2072E+11	-104.54	-96.19	-79.57	0.00	-105.24	-94.38	-91.39	-95.78	-86.27	-96.34	-96.60	-92.39	ADC3	-86.17
6.2062E+11	-101.05	-92.37	-99.34	-90.59	0.00	-81.02	-98.27	-96.13	-84.93	-98.46	-85.31	-91.32	ADC4	-86.17
6.1992E+11	-90.13	-94.49	-94.75	-92.17	-76.53	0.00	-87.73	-88.65	-93.01	-91.38	-93.50	-97.63	ADC5	-86.16
6.2074E+11	-93.36	-97.23	-87.30	-90.33	-93.46	-91.74	0.00	-82.17	-85.03	-92.92	-92.57	-99.32	ADC6	-86.17
6.2142E+11	-90.58	-92.62	-89.87	-95.18	-110.37	-91.97	-78.80	0.00	-88.62	-90.71	-87.55	-100.82	ADC7	-86.17
6.1656E+11	-92.42	-98.34	-98.30	-90.07	-94.73	-109.80	-105.18	-91.19	0.00	-78.53	-92.84	-95.89	ADC8	-86.14
6.2279E+11	-88.44	-101.86	-88.71	-92.94	-96.92	-97.50	-95.45	-101.70	-80.30	0.00	-92.77	-94.70	ADC9	-86.18
6.2136E+11	-102.88	-97.28	-101.09	-95.86	-98.97	-97.66	-91.15	-105.56	-89.59	-83.91	0.00	-79.76	ADC10	-86.17
6.1719E+11	-97.54	-93.85	-97.70	-92.31	-93.85	-95.18	-97.58	-97.93	-92.74	-85.53	-77.97	0.00	ADC11	-86.14
12.2 MHz/10.000V test signal, +95/-96 digital level														
6.1460E+11	0.00	-88.33	-87.73	-97.11	-92.51	-105.33	-95.13	-97.08	-91.27	-91.13	-95.03	-103.50	ADC0	-86.12
6.1397E+11	-86.91	0.00	-91.53	-92.58	-98.05	-95.90	-96.98	-95.09	-96.23	-100.16	-89.61	-96.84	ADC1	-86.12
6.1280E+11	-95.88	-96.41	0.00	-91.75	-94.27	-101.83	-89.97	-102.09	-92.90	-101.12	-92.27	-97.38	ADC2	-86.11
6.1612E+11	-94.54	-98.66	-86.58	0.00	-94.40	-98.42	-95.28	-98.18	-105.55	-100.90	-86.07	-93.39	ADC3	-86.14
6.2237E+11	-91.47	-94.15	-92.46	-90.71	0.00	-89.92	-95.44	-107.13	-99.59	-98.34	-91.32	-95.43	ADC4	-86.18
6.1937E+11	-94.92	-98.23	-95.86	-96.35	-86.17	0.00	-91.47	-92.86	-90.93	-92.16	-96.52	-90.82	ADC5	-86.16
6.1588E+11	-95.38	-98.60	-95.25	-87.58	-108.31	-91.87	0.00	-87.19	-93.79	-93.55	-87.93	-90.03	ADC6	-86.13
6.1913E+11	-92.76	-95.00	-90.68	-89.65	-95.62	-90.84	-89.92	0.00	-98.18	-92.80	-87.47	-91.05	ADC7	-86.16
6.1776E+11	-93.84	-100.21	-97.21	-95.32	-92.20	-100.50	-95.58	-97.51	0.00	-84.92	-88.59	-92.83	ADC8	-86.15
6.2119E+11	-93.80	-100.60	-94.69	-96.81	-94.00	-92.35	-94.39	-104.33	-88.32	0.00	-96.58	-90.55	ADC9	-86.17
6.1763E+11	-102.67	-89.40	-94.95	-92.31	-103.49	-96.54	-105.18	-93.50	-91.89	-87.33	0.00	-85.81	ADC10	-86.15
6.1457E+11	-90.54	-92.49	-92.70	-93.49	-105.07	-96.09	-98.93	-97.60	-90.09	-104.92	-92.16	0.00	ADC11	-86.12
4.8 MHz/10.000V test signal, +83/-84 digital level														
4.6369E+11	0.00	-100.16	-81.27	-85.89	-92.98	-90.42	-97.79	-103.03	-82.95	-104.48	-84.55	-89.73	ADC0	-84.90
4.6319E+11	-93.36	0.00	-85.11	-89.61	-84.43	-96.91	-84.93	-90.41	-82.84	-91.13	-83.59	-86.84	ADC1	-84.90
4.5783E+11	-86.33	-78.60	0.00	-84.22	-85.59	-82.07	-87.74	-98.58	-87.17	-95.32	-80.04	-104.78	ADC2	-84.85
4.6318E+11	-97.32	-80.45	-83.25	0.00	-92.04	-102.29	-87.21	-85.75	-80.66	-86.32	-81.84	-98.93	ADC3	-84.90
4.6991E+11	-84.56	-87.80	-88.96	-85.50	0.00	-81.06	-87.02	-92.71	-85.12	-86.10	-81.48	-84.71	ADC4	-84.96
4.6873E+11	-89.94	-85.15	-84.37	-85.70	-88.48	0.00	-102.39	-87.06	-79.74	-93.47	-80.41	-86.66	ADC5	-84.95
4.6134E+11	-82.10	-86.29	-87.88	-88.20	-97.89	-84.49	0.00	-80.11	-81.80	-91.07	-81.82	-82.89	ADC6	-84.88
4.6820E+11	-92.08	-90.03	-87.23	-85.77	-81.59	-92.75	-88.66	0.00	-81.97	-101.21	-82.64	-80.84	ADC7	-84.94
4.6550E+11	-95.70	-90.66	-88.05	-84.71	-85.45	-85.97	-84.40	-87.68	0.00	-80.80	-77.80	-81.68	ADC8	-84.92
4.6997E+11	-90.57	-100.82	-97.59	-85.73	-93.25	-87.38	-86.19	-87.78	-83.11	0.00	-80.88	-88.88	ADC9	-84.96
4.6479E+11	-105.18	-92.84	-94.96	-85.09	-94.46	-96.90	-82.39	-86.06	-77.21	-85.08	0.00	-85.85	ADC10	-84.91
4.6417E+11	-86.08	-87.20	-86.22	-92.76	-85.36	-87.02	-86.21	-90.63	-78.87	-82.32	-78.89	0.00	ADC11	-84.91

The values in the above table were obtained in the following way: of the 8192 FFT channels, exactly one channel corresponds to the test frequency. At each test frequency, for each ADC, the power in the channel corresponding to the test frequency was obtained by taking the squared magnitude of the FFT in the channel. The power ratio x of [test signal : observed power in channel] was then obtained, and converted to dB as $10log_{10}(x)$. Since the ratio of the test signal to itself is 1, its $\log_{10}$ is 0, thus the diagonal entries of zeroes correspond to the ADC receiving the test signal in each test case.

The rightmost column gives 3x the average observed power in frequency channels near the test signal. Since the frequencies of the test signal and dithering signal were carefully chosen as described in the test setup section, these channels should contain no component of any input

signal. Therefore, the average noise power should be due solely to quantization noise. This means any signal higher than this average level could be a crosstalk spur; however, the noise power was manually calculated and is not averaged in the data, so the observed power at a particular frequency in any one channel could be higher or lower. The observed power from quantization noise at any one frequency is unlikely to be more than 3x the average, so this figure is used as a rough estimate for the power level at which a spur can be confidently characterized as crosstalk. Conversely, if no spur higher than 3x the average noise power is detected in a particular ADC channel, then that channel is characterized as having no measurable crosstalk. In the table, ADC channels exhibiting measurable crosstalk are colored in red, while the channel with the highest noise power in each column is underlined.

In most cases the testing apparatus seems to be sensitive enough to measure crosstalk down to the -86 dB level. For 97.6 MHz, sensitivity to only -80 dB is observed because the Rigol generator has less power available above 50 MHz, and therefore transmitted only a 5V signal instead of the 10V in other test cases. A tabular summary of test results is included below:

Test Frequency	*Crosstalk Threshold*	*Crosstalk, Same Chip*	*Crosstalk, Other Chips*
4.88 MHz	-84.9dB	• -77 dB max • most below -80 dB	-80 dB max
12.207 MHz	-86.2dB	No case has crosstalk above the threshold.	No case has crosstalk above the threshold.
48.828 MHz	-86.2dB	• -76 dB max • adjacent ADCs ~ -80 dB, • all others below threshold	Other chips: all below threshold.
97.656 MHz	-80 dB	• adjacent ADCs -71 to -75 dB • all others below threshold	Other chips: all below threshold.

These figures for crosstalk between ADC channels show fairly promising results across the SNAP board. The HMCAD1511 is rated as having a typical crosstalk of -70dBc at a test signal frequency of 70MHz and full-scale power. No figures worse than that level are observed here. Crosstalk in adjacent channels has a power ranging roughly from -71 to -85 dBc, telling us that the ADC chips are performing to spec. Perhaps the most interesting result from these tests is that it appears that the SNAP board itself is not acting as a bottleneck on analog-to-digital conversion performance. Because the total observed cross talk is less than that claimed for the HMCAD1511, assuming measured cross talk is due to the chip, there is none from the board layout (e.g. non-ideal effects from baluns, parasitics from board layout, etc.) that we are able to measure.

Future Work

The results from these tests show that to first order, the SNAP board layout is not a limiting factor in minimizing crosstalk between channels, and that the ADCs are operating within spec. However, more testing is necessary to fully characterize ADC performance. A different quad ADC chip[5] from Texas Instruments with typical adjacent crosstalk rating of -90dBc may be

[5] http://www.ti.com/lit/ds/symlink/ads58c48.pdf

used for the next LWA design. Several improvements to this testing method could be made to test this new chip's performance more comprehensively.

In order to test crosstalk at levels more sensitive than -70dBc and verify that the SNAP board will not bottleneck this higher-performing new chip, one option would be to obtain a series of frequency spectra and average the power in those spectra in the FPGA for a smoother spectrum with less fluctuation in noise power.

Another improvement currently in development is an FPGA implementation of a polyphase filter bank for the Xilinx XC7K160T FPGA onboard the SNAP. Because it would inherently minimize the effects of DFT leakage and scalloping loss, this FPGA-based polyphase filter bank will allow us to test ADC performance without placing test signals at the center of FFT bins or carefully interpolating the dither frequency before performing tests.

Finally, pushing the FPGA hardware to its limits in order to implement an FFT with more than 8192 channels would give better frequency resolution and sensitivity. Implementing any or all of these test improvements should allow for a more effective analysis of the gravity and causes of observed spurious responses and other non-idealities from the ADCs.