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LWA352 Digitizers: Design Concept

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I. INTRODUCTION

The first stage of digital signal processing for LWA352 will use SNAP2 FPGA boards [1]. Each SNAP2 is expected to be capable of handling at least 64 LWA signals sampled at about 200 MHz, but it is a challenge to get that many digitized signals into the board. Our design will achieve this by using both of the SNAP2's FPGA Mezzanine Card high-pin-count (FMC-HPC) connectors to accommodate daughter cards carrying the analog-to-digital converters. It is the design of those Digitizer Boards that we discuss here..

II. CONSTRAINTS

Analog signal processing for LWA352 will be accomplished in a separate rack from the digital processing, and each signal will be connected to the digital rack on a coaxial cable. Available ADC integrated circuits for our sampling rate have differential inputs, so baluns is required on the Digitizer Boards.

A survey of available ADC ICs identified only two devices having at least 4 channels and at least 8 bits of resolution at 200 MHz sampling: the Analog Devices HMCAD1511 and the Texas Instruments ADS5296A. The HMCAD1511 has been used in some Casper ADC boards [2], including those of the first- and second-phase implementations of LWA-OVRO. We have selected the ADS5296A because it claims better isolation among channels, has finer resolution (10b), and has additional useful features (including synchonization among devices and register readback).

The FMC interface is a VITA/ANSI industry standard [3] that specifies the connectors in some detail, including functional assignments of pins [4]. The SNAP2 closely conforms to the standard pinout, although some pins are unconnected. The standard also specifies the form factor and other details of the daughter ("mezzanine") cards [5], making them rather small; all are 69 mm wide and the longest is 84 mm. This is not enough space for a large number of coax connectors, balun transformers, and ADC ICs. To get 64 signals into the SNAP2, we need 32 per FMC connector, requiring 8 of the ADS5296A quad-ADC devices. We will use a non-standard form factor, but the width is still constrained by the spacing of the connectors on the SNAP2 board (Figure 1) to a maximum of 76 mm. The SNAP2 is designed to fit a standard FMC card that is 76.5 mm long, but ours will have to be longer, so they will extend over the front edge of the SNAP2.

III. CONCEPT

A. Board Stacking

Even with a board that is 76 mm wide by 127 mm long (extending 51 mm beyond the edge of SNAP2), it is impossible to accommodate 32 signals. (Note that the Casper ADC16-250 ADC boards [2] are 86 mm wide and 127 mm long and handle 16 signals.) Our design involves stacking two boards, each handing 16 signals, onto each FMC connector of SNAP2. The lower board will have an FMC-HPC "mezzanine" connector on one side, mating with the SNAP2's "carrier" connector, and an FMC-HPC carrier connector on the other side, mating with a mezzanine connector on the upper board. See Figure 2. The two boards will use distinct sets of FMC connector pins for their respective digitized signals, but will share the same pins for power and control.
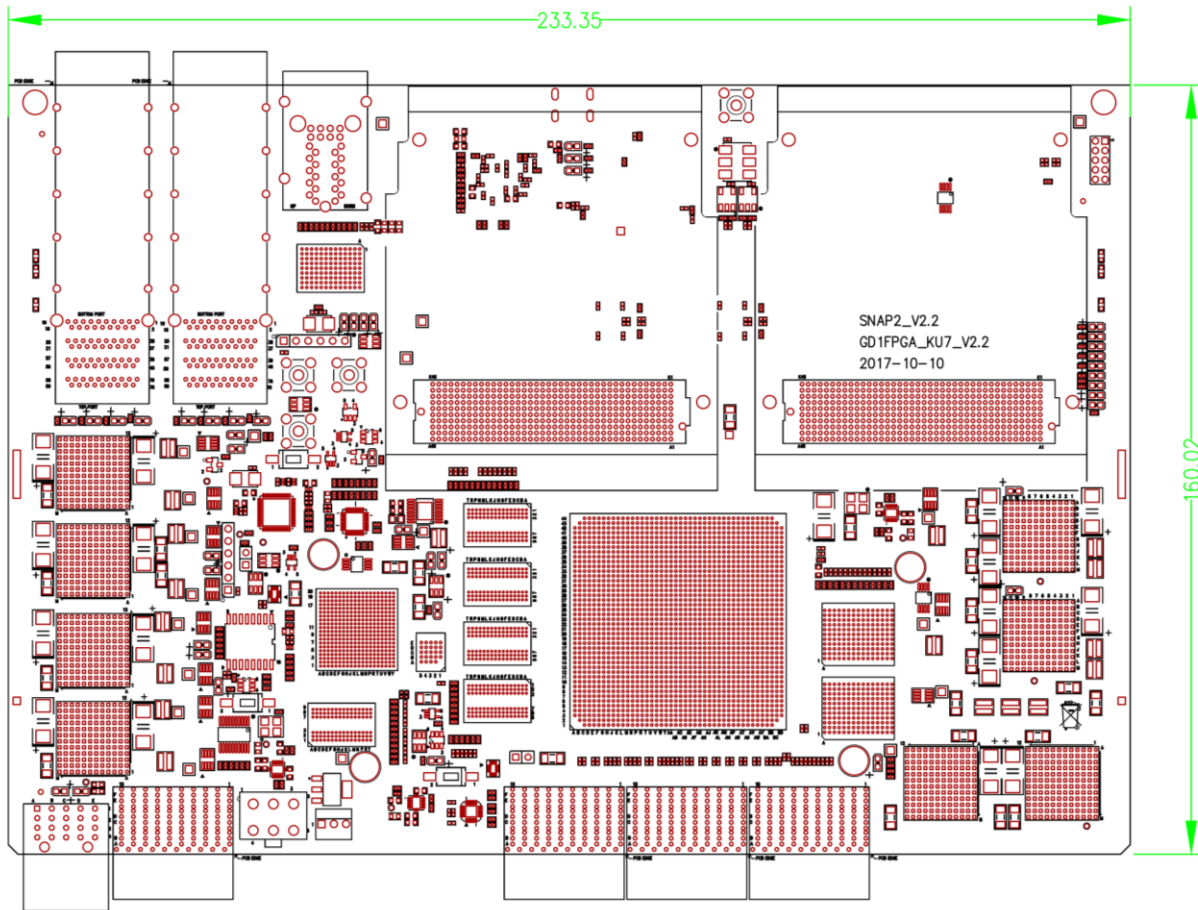
Figure 1. Top view of SNAP2 board, showing silkscreen layer. We are calling the top edge of this figure the "front." Space for two FMC cards is in the upper right quadrant, with the outlines shown for 76 mm x 76.5 mm boards conforming to one of the FMC-standard form factors. Our boards will be wider and longer.

Board stacking is *not* included in the FMC standard. There was initially some concern that signal integrity might not be adequate for the upper board, since its signals must pass through two additional connectors and the lower board on their way to the SNAP2, even though a standard FMC connector pair is specified to handle LVDS signaling at up to 10 Gb/s and our signals are at less than 1 Gb/s. To check this, we constructed an "FMC Test Board" and used it to demonstrate error-free signaling at 1.25 Gb/s between an available ADC board and a SNAP2 [6].

Because of their different connections to FMC pins, the upper and lower boards will need different PCB layouts and separate board fabrications, but except for the routing to the FMC connectors, both boards can be the same. They can have identical bills of materials and the placement of all parts can be identical, except that on the upper board the FMC carrier connector can be omitted. Assembly of all boards can be done in a single run[1].

B. Components and Circuits

To fit 16 coax inputs onto the board, it is necessary to use small connectors. MMCX connectors were chosen. They take up less board space and can be packed closer together than

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[1] The LWA352 system requires 44 Digitizer boards, 22 lower and 22 upper, and 11 SNAP2 boards. We are planning a production run of 50 boards, 25 of each variety, to provide some spares.
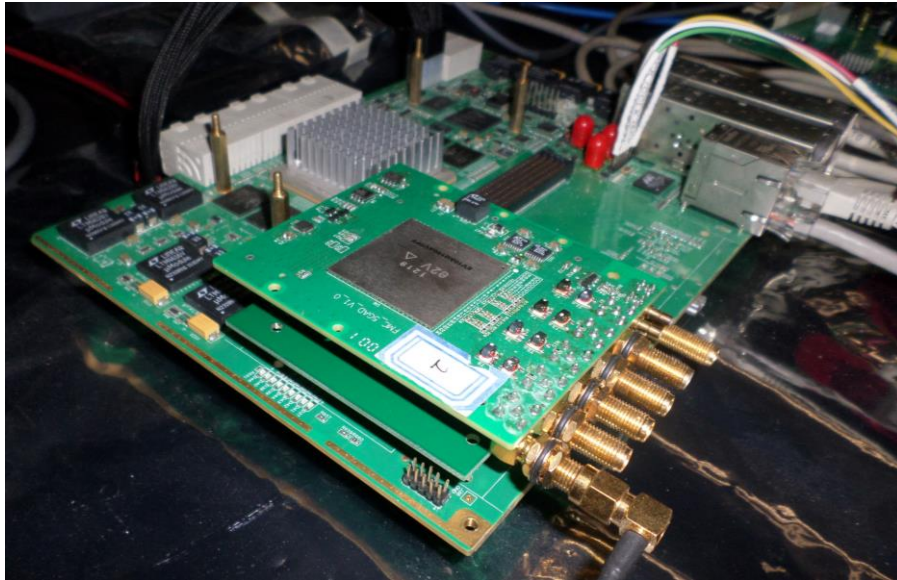
Figure 2. SNAP2 with FMC Stacking Test Board [6] and 5GAD mezzanine board stacked on the left-hand FMC connector.

SMA or SMB, and their construction allows them to have less leakage than other push-pull connector types.

The main components on each board are four ADS5296A quad-ADC ICs, each handling 4 signals. The circuitry surrounding all ADS5296As is identical, as shown in Figure 3. A major objective of the design is to achieve the highest possible isolation among the analog signals. A balun transformer is placed adjacent to each input connector. Importantly, the outer conductor of the coax is not connected to board ground, but only to one side of the transformer primary. Common-mode DC bias is provided through the center tap of the transformer secondary, with heavy LC isolation of the bias circuits from each other. Digitized samples are sent to the FMC connnector using 8 LVDS pairs per ADC device, each running at 5 times the sampling clock, or about 1.0 Gb/s in our system. See the ADS5296A data sheet for details. We thus need a total of 32 such LVDS output signals per board. Each ADS5296A also provides two clocks synchronous with its output data: a DDR bit clock and a sample (word) clock. We do not have enough FMC pins to send all of these to the FPGA, but not all are needed since the clocks from all ADC ICs are at the same frequencies. We transmit the bit clock from one of the ADS5296As and the sample clocks from two of them.

The board must also have common circuitry to provide DC power, clock distribution, and control.

The SNAP2 provides power via the FMC connector at 12V (or 5V, depending on jumpers), 3.3V (3P3V), and 1.8V (VADJ). All circuitry on the Digitizer board operates at 1.8V, but the ADC chips have separate power for their analog and digital sides. To keep the analog 1.8V power as clean as possible, we use a linear regulator driven by 3.3V from SNAP2. For the 1.8V digital power, we include a separate linear regulator driven by 3.3V, but we also provide a jumper-selected option to use the SNAP2's 1.8V directly. To minimize power consumption, it is preferred to use the 1.8V directly, but we have some concern about noise because the SNAP2 produces 1.8V via switching DC-to-DC converters. Having the on-board regulator also allows the Digitizer Board to be used with a carrier other than SNAP2 that might not provide 1.8V; all FMC carriers should provide 3.3V.
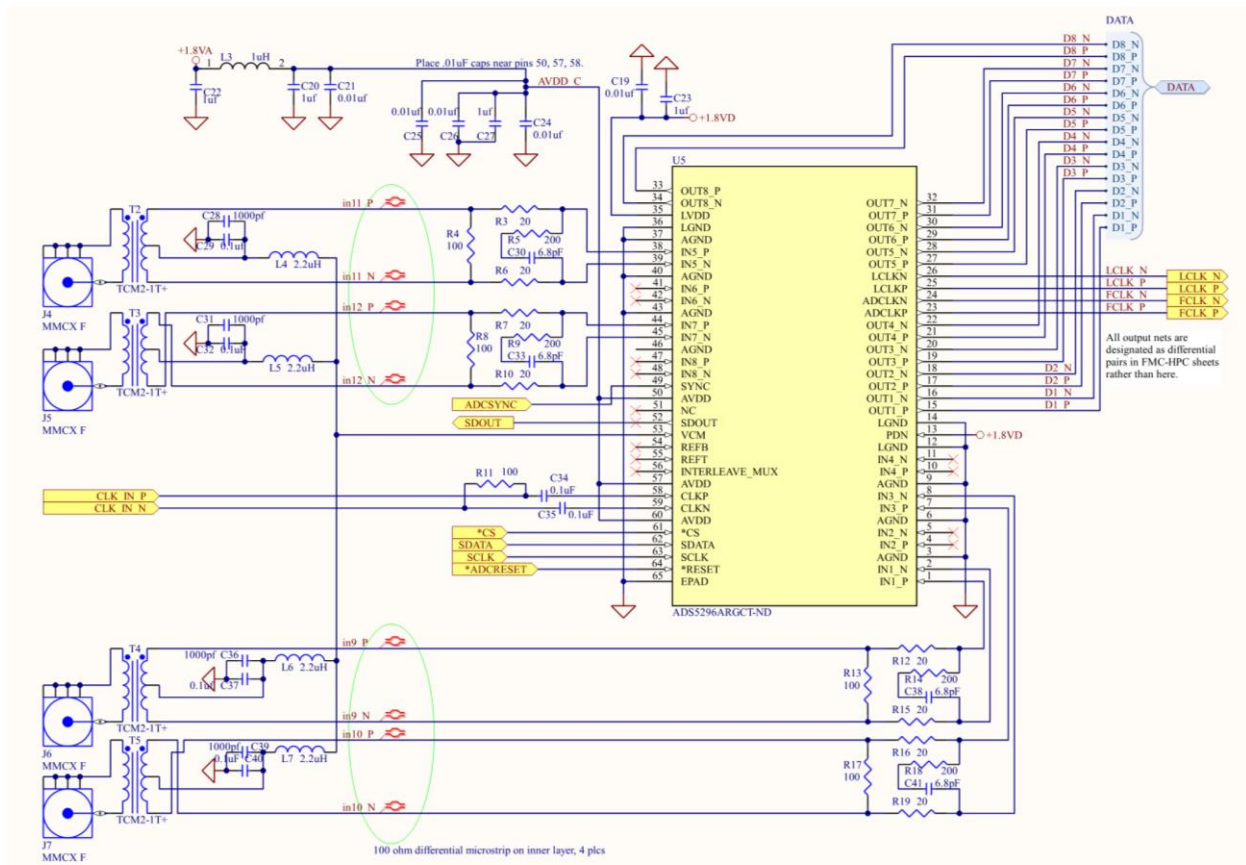
Figure 3. Schematic of the circuitry associated with one of the ADS5296A ADC ICs on the new Digitizer Boards.

A clock signal is provided to the board at the sampling frequency (about 200 MHz for LWA) on an SMA connector. A 1:4 clock distribution IC is used to send a copy of the clock to each ADC IC. The ADCs and the clock distributor use differential signaling, so a balun is required at the SMA connector.

Control of the ADCs uses an SPI serial bus from the FPGA via the FMC connector. See the ADS5296A data sheet for details. The SPI signals are common to both boards of our stack. SPI uses chip-select signals to address each device separately; a 3-bit chip select code is decoded on the Digitizer Board, with the MSB used to select the upper or lower board of the stack.

C. Placement and Routing

To minimize cross-talk and RFI pickup in the analog signals, the input connectors should be spread out as much as possible. Both sides of the board can be used. See Figure 4. Magnetic coupling among the balun transformers can occur, so their placements and orientations should be chosen to minimize it. A 100-ohm differential transmission line connects each balun to input pins of the ADC; these should be differential stripline, with the signals on an inner layer.

Data and clock outputs, as well as the clock input, use differential signaling on 100-ohm transmission lines. These will probably need to use both inner and outer copper layers, as differential stripline and differential microstrip, respectively.

Although the board width is limited to 76 mm, the length can be increased as needed to provide space for components and routing.

The board is expected to require at least 8 copper layers, including planes for ground and
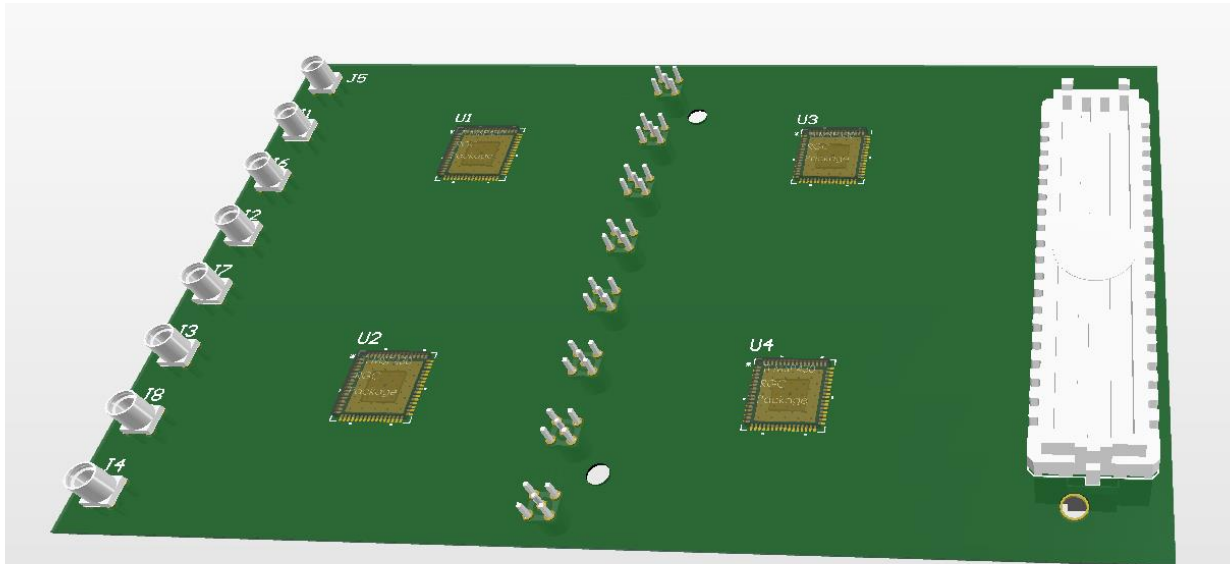
Figure 4. Possible placement of major components, including input MMCX connectors and ADS296A ADC ICs. This board is 127 mm long by 76 mm wide.

power. Expansion to 10 layers can be considered if necessary.

D. Support of Other Carriers, Including LPC

To maximize the long-term usefulness of our design, it is desirable to provide compatibility with FPGA carrier cards other than SNAP2 Many FMC carrier cards are available commercially, and others may be built for special purposes, like SNAP2. Since our design conforms electrically to the FMC standard, it should be immediately compatible with many other carrier boards. However, it does not conform to the standard mechanically, so it can only be fully compatible with carriers that have enough space for its larger horizontal size. Also, some carriers do not have connections to all FMC signal pins and some use pins in non-standard ways.

The FMC-HPC connector has 400 pins, which is sufficient to support our two stacked 16-signal boards, but the standard also provides for a low-pin-count connector (FMC-LPC) with 160 pins. Some carriers have only an FMC-LPC connector, especially if they have a small FPGA with limited I/O pins. The FMC-HPC and FMC-LPC connectors are mechanically the same, so they can be inter-mated.. Our design chooses the FMC pin assignments for the upper board so that it can work with an LPC carrier, although there are some restrictions. There are not enough pins to deliver any of the sample (frame or word) clocks, just one bit clock, nor to support the synchronization signal or the register readback signal.

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