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FMC Daughter Board Stacking on SNAP2: Signal Integrity Tests For LWA352 Digitizers

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FMC Daughter Board Stacking on SNAP2: Signal Integrity Tests For LWA352 Digitizers

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I. Introduction

The digital processing design for LWA352 includes use of SNAP2 FPGA boards [1] for the initial processing stage, including the F engine and cosmic ray detection. Calculations and benchmarking show [2] that the Xilinx Ultrascale XCKU115FLVF1924 FPGA on the SNAP2 board has sufficient processing and I/O capacity to handle at least 64 separate signals. However, creating enough digitizer channels to accept 64 analog signals and to deliver their quantized samples to the SNAP2 is challenging. ADC chips capable of nearly 200 MHz sampling rate can handle at most 4 signals each, so 16 such chips are needed. On the analog side, connectors for delivering those signals to the ADCs necessarily occupy significant PCB area, especially since they must be kept well separated to avoid cross-talk.

For available ADC chips, the digitized output is provided via multiple high-speed LVDS streams. For such signals, the most suitable digital interface from digitizer boards to the SNAP2 is the FPGA Mezzanine Card (FMC) connector. The SNAP2 has two high-pin-count FMC connectors, each with 400 pins. We have verified that each of these has sufficient LVDS pairs routed to the FPGA to support 32 signals. The FMC concept is that a daughter board ("mezzanine card") plugs into the mother board ("carrier card"). Figure 1 includes a photograph of a SNAP2 board showing its two FMC connectors with no mezzanine cards, and with a card plugged into the "left" connector. That mezzanine card (from the Chinese Institute of Automation, IoA) has size 69.0 x 84.2 mm and fits within the space allowed for it on the SNAP2.

There are standard form factors for FMC-compliant mezzanine cards, but we are designing our own digitizer boards and we are not constrained to use those form factors. Nevertheless, the SNAP2 layout limits the width of FMC cards to 76 mm if both connectors are used. The length can be considerably larger than that of the card shown in Fig 1 if we are willing to have it cantilevered beyond the edge of the SNAP2. We will do that for our boards.

With these constraints, we find that we are unable to handle more than 16 signals on a single digitizer board, even when it is constructed as a 10-layer board. A preliminary rendering of such a board is shown in Figure 2. It uses 16 MMCX coax connectors for its analog inputs, and 4 Texas Instruments ADS5296A quad-ADC chips. To deliver 32 digitized signals to one FMC connector, we plan to stack two such boards, with the upper and lower boards using different FMC pins for their output LVDS streams and clocks but common pins for power and control. The lower board requires an FMC carrier-card connector on its upper side and an FMC mezzanine-card connector on its lower side, with selected pins connected directly from one side to the other.

A concern with this arrangement is whether the integrity of the high-speed LVDS signals can be maintained across two mated FMC connector pairs and through the lower board. This report describes tests that demonstrate satisfactory performance in that situation.

II. Methods

We built a special "FMC Stacking Test Board" (Figure 3) that has a mezzanine-card FMC connector on one side, a carrier-card FMC connector on the other side, and with all corresponding pins tied together through vias on the board. A few pins are also broken out for

laboratory testing.

We have on hand a "5GAD" board from IoA (Fig 1). It is a high-speed digitizer capable of up to 5 GSa/s for a single signal or 1.25 GSa/s for each of 4 signals and is based on the EV10AQ190A chip made by e2v [3]. This is the only SNAP2-compatible FMC card that we have available, but it uses multiple fast LVDS streams for its output interface and allows robust tests of the signal integrity across that interface.

The test consists of verifying that we can get error-free data capture into the FPGA with the 5GAD board plugged directly into each of the SNAP2's FMC connectors, and then to verify that we also get error-free data capture with the FMC Stacking Test Board inserted between the 5GAD and the SNAP2 (Figure 4). To accomplish this, one of us (JH) created FPGA code that puts the ADC chip into a test mode where its output is a known pattern (rather than digitizing its analog inputs) and checks the captured data against that pattern, counting errors. This code is a modified version of a Vivado project provided by IoA. The IoA code includes a state machine, run during initialization, that optimizes the data capture by adjusting the clock phase.

The EV10AQ190A chip includes 4 ADC cores, each of which operates independently from a common externally-supplied clock. The sampling rate of each core is 1/2 of the external clock frequency. For each sample, each core delivers a 10b digitized value and an overrange bit in parallel on 11 LVDS pairs. Each core also provides a DDR output clock on another LVDS pair 1/2 the sampling rate, but only the clock for core A is connected across the FMC to the FPGA. The data sheet gives the external clock range as 0.7 to 2.5 GHz; thus, at the maximum speed, the sampling rate is 1.25 GHz, the data rate for each of the 44 LVDS signals is 1.25 Gb/s, and the output clock frequency is 625 MHz.

The code uses the chip's "ramp" test mode in which the sample value, treated as an unsigned 10b integer, is incremented on each sample. For each core, the FPGA de-multiplexes the streams by a factor of 8, delivering 8 successive samples in parallel to internal logic operating at 1/8 of the sample rate (156.25 MHz maximum). The code checks that the 8 samples form a ramp, and that the each of them is 8 more than the corresponding sample of the previous group of 8. If so, it increments an "OK" counter; otherwise it increments an "error" counter. This is done separately for each core, and then the counters are summed across the 4 cores. The counters are cleared during initialization, after which they operate continuously. The sum registers can be read by software at any time via the SNAP2's JTAG bus. A script has been written to read and display the results every 6 seconds.

III. Results

Four tests were performed, each in the same way:

- 5GAD board (alone) on right-hand FMC connector
- 5GAD board on Stacking Test Boad on right-hand FMC connector
- 5GAD board (alone) on left-hand FMC connector
- 5GAD board on left Stacking Test Boad on right-hand FMC connector.

Each test consisted of setting the external clock synthesizer (a Hittite HMC2220) to 2.0 GHz at 0 dBm, running the script (which programs and initializes the FPGA, including optimizing the capture clock phase and clearing the counters), and then increasing the clock frequency by 0.1 GHz approximately every 60 s. The script output was then analyzed.

The results were the same for all 4 tests. No errors were detected at clock frequencies of 2.0 to 2.5 GHz, but at 2.6 GHz the error rate was 100%.

An example of a few lines of the script output text is shown in Listing 1. Every 6s, the

time, total errors, total OK, and number of samples since the previous line are printed. (The latter is not quite constant because the 6s interval is determined by a software timer that is not exact.) At the beginning of this listing, the test had already been running for 5 minutes; no errors had been detected, but a large number of 'OK' results were counted. Each OK count means that there were no errors in a group of 8 samples from each core. The number of samples is given by 8(*de* + *do*), where *de* and *do* are the differences in the error and OK counts from the previous line. The error rate during that interval is then *de*/(*de* + *do*). At the beginning of the listing, the clock frequency was 2.4 GHz. Between 15:49:31 and 15:49:37 it was increased to 2.5 GHz, and between 15:50:31 and 15:50:37 it was increased to 2.6 GHz. It can be seen that the error rate became 100% at 2.6 GHz.

IV. Discussion

Out interest here is in verifying the integrity of the FMC data interface when two mezzanine boards are stacked. The test has achieved that up to a clock rate of 2.5 GHz, which corresponds to a data rate of 1.25 Gb/s across each of 40 LVDS pairs (10b per core). In our application for LWA352, the data rate needed across the interface is 0.8 or 1.0 Gb/s (for the 8b HMDAC1511 or 10b ADS5296A quad-ADC chip, respectively). We can therefore be confident that performance of the interface will be satisfactory.

The failure at and above 2.6 GHz clock frequency is curious. The data sheet of the EV10AQ190A [3] does specify a maximum clock rate of 2.5 GHz, but this includes achieving all of its analog-side digitization accuracy specs. Since our test does not use any of the analog side but only its internal logic, we expect it to work for some margin above 2.5 GHz. The fact that the error rate goes abruptly to 100%, rather than to some lower non-zero rate[1], suggests a failure of the chip's logic rather than of the data capture interface. This is further suggested by some other observations in our tests: Once errors start occurring, reducing the clock speed well below 2.5 GHz does not restore error-free operation; the error rate continues at 100%. Starting the test at 2.5 GHz, so that the capture clock optimization is done at that speed rather than at 2.0 GHz, makes no difference; the error rate still goes to 100% at 2.6 GHz. Starting at 2.6 GHz results in 100% error rate immediately.

References

[1] Jie Hao, Qiuxiang Fan, Liangtian Zhao, Jingbin Mu, Hui Feng, amd Lin Shu, "Design of the Snap2 System." Institute of Automation, Chinese Academy of Sciences. (Undated, approximately November 2015.

[2] Jonathon Kocz and Kathrlyn Plant, "Digital Subsystem." Presentation to LWA-352 Preliminary Design Review meeting, 2015 June 17-18.

[3] Teledyne e2v Semiconductors, "EV10AQ190A, Low power QUAD 10-bit 1.25 Gsps ADC Operating up to 5 Gsps." Datasheet DS1070, October 2019. https://www.teledyne-e2v.com/content/uploads/2019/10/EV10AQ190A_1070C.pdf

[1] In an early test (2020 Jan 27), starting at 2.6 GHz clock, error-free operation was achieved up to 2.9 GHz and an error rate of 18.2% ± 1.2% was observed at 3.0 GHz. This is more consistent with the errors occurring at the interface. But in spite of multiple attempts, that result could not be repeated.

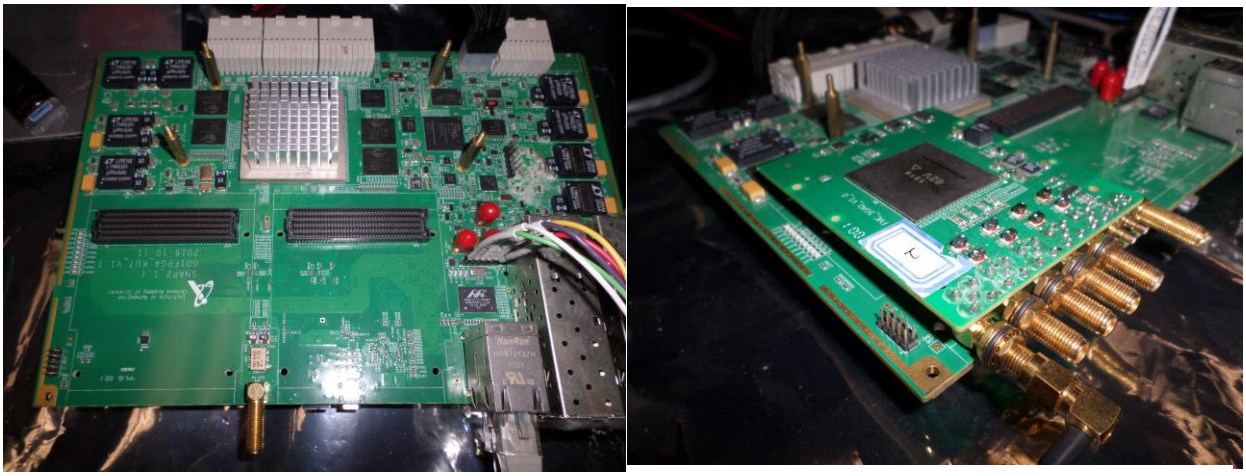

Figure 1. *Left:* SNAP2 board showing its two HPC FMC connectors. *Right:* SNAP2 with a 5GAD mezzanine card plugged into the left-hand FMC.

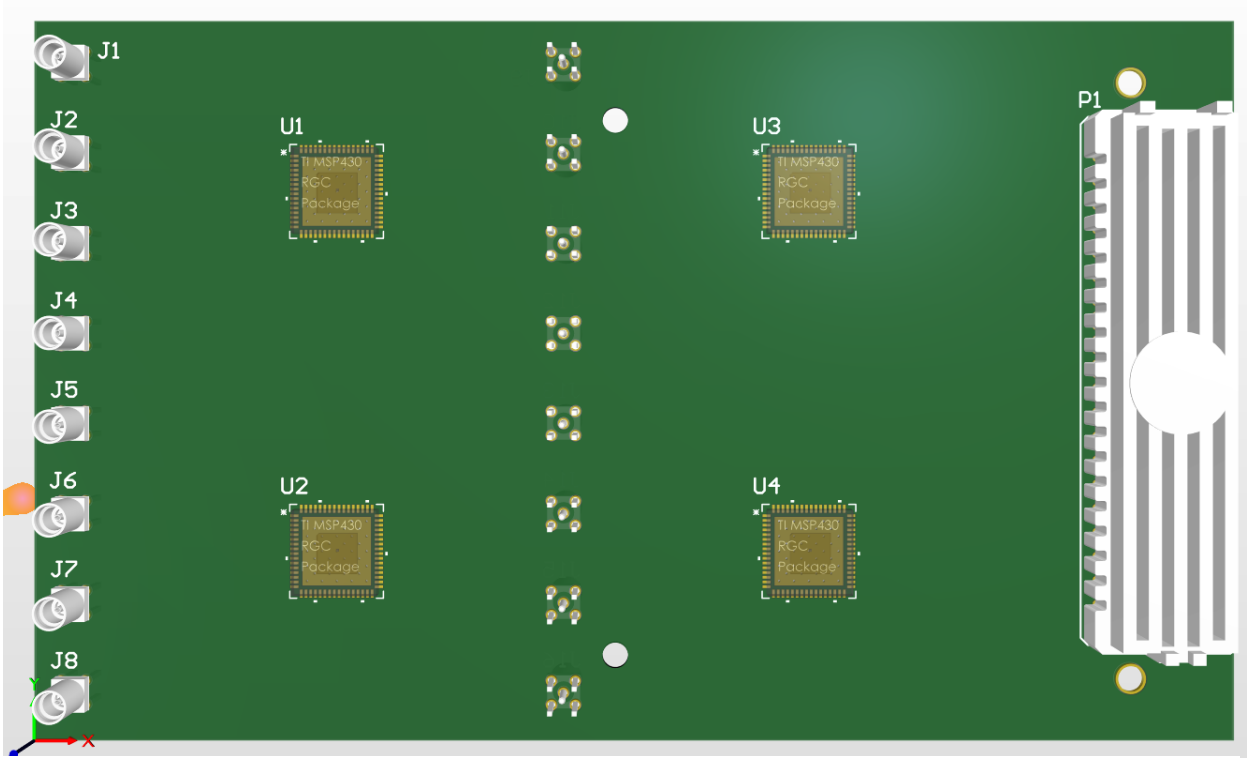

Figure 2. Rendering of preliminary layout of a 16-signal FMC digitizer board. Its size is 127x76 mm. This is the bottom view, with the FMC mezzanine card connector (P1) on the right. Eight of the MMCX coax input connectors are on the left, and the other 8 are in the middle on the top side. Four ADS5296A ADC chips are shown (U1-U4). For the version on the bottom of the stack, the top side includes an FMC carrier card connector, just above P1.

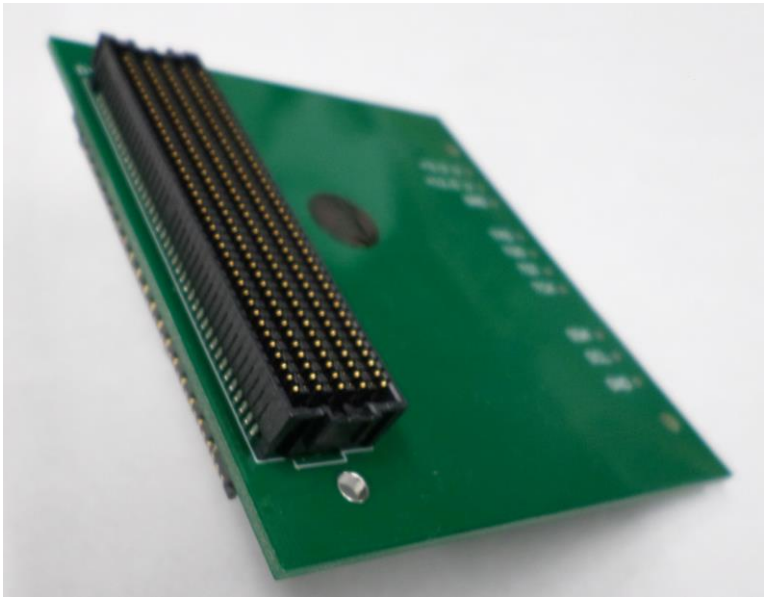

Figure 3. FMC Stacking Test Board with carrier connector on top side (shown) and mezzanine connector on bottom.

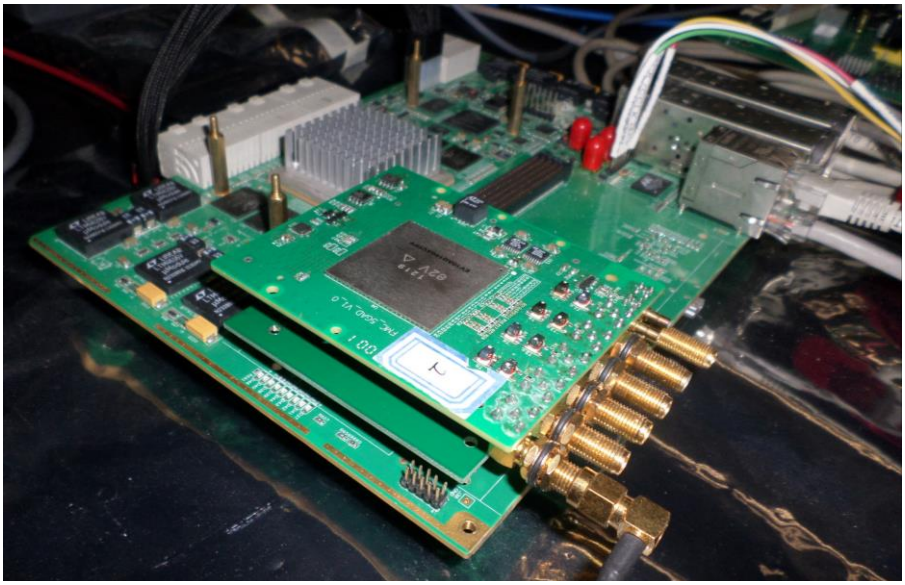

Figure 4. SNAP2 with FMC Stacking Test Board and 5GAD mezzanine board stacked on the left-hand FMC connector.

Listing 1: Script Output, Test 2020/01/29b, Left FMC With Stacking Test Board

```
2020-Jan-29 15:49:13: Errors: 0. OK: 165888200172 (28.835837632 GSa)
2020-Jan-29 15:49:19: Errors: 0. OK: 169494645500 (28.851562624 GSa)
2020-Jan-29 15:49:25: Errors: 0. OK: 173099463028 (28.838540224 GSa)
2020-Jan-29 15:49:31: Errors: 0. OK: 176705894304 (28.851450208 GSa)

2020-Jan-29 15:49:37: Errors: 0. OK: 180385937156 (29.440342816 GSa)
2020-Jan-29 15:49:43: Errors: 0. OK: 184140979676 (30.04034016 GSa)
2020-Jan-29 15:49:49: Errors: 0. OK: 187896206012 (30.041810688 GSa)
2020-Jan-29 15:49:55: Errors: 0. OK: 191653679716 (30.059789632 GSa)
2020-Jan-29 15:50:01: Errors: 0. OK: 195410309896 (30.05304144 GSa)
2020-Jan-29 15:50:07: Errors: 0. OK: 199164698916 (30.03511216 GSa)
2020-Jan-29 15:50:13: Errors: 0. OK: 202920115856 (30.04333552 GSa)
2020-Jan-29 15:50:19: Errors: 0. OK: 206675475880 (30.042880192 GSa)
2020-Jan-29 15:50:25: Errors: 0. OK: 210432333748 (30.054862944 GSa)
2020-Jan-29 15:50:31: Errors: 0. OK: 214189481112 (30.057178912 GSa)

2020-Jan-29 15:50:37: Errors: 1820580420. OK: 216195974796 (30.616592832 GSa)
2020-Jan-29 15:50:43: Errors: 5729114736. OK: 216195974796 (31.268274528 GSa)
2020-Jan-29 15:50:49: Errors: 9636980960. OK: 216195974796 (31.262929792 GSa)
2020-Jan-29 15:50:55: Errors: 13582226076. OK: 216195974796 (31.561960928 GSa)
```